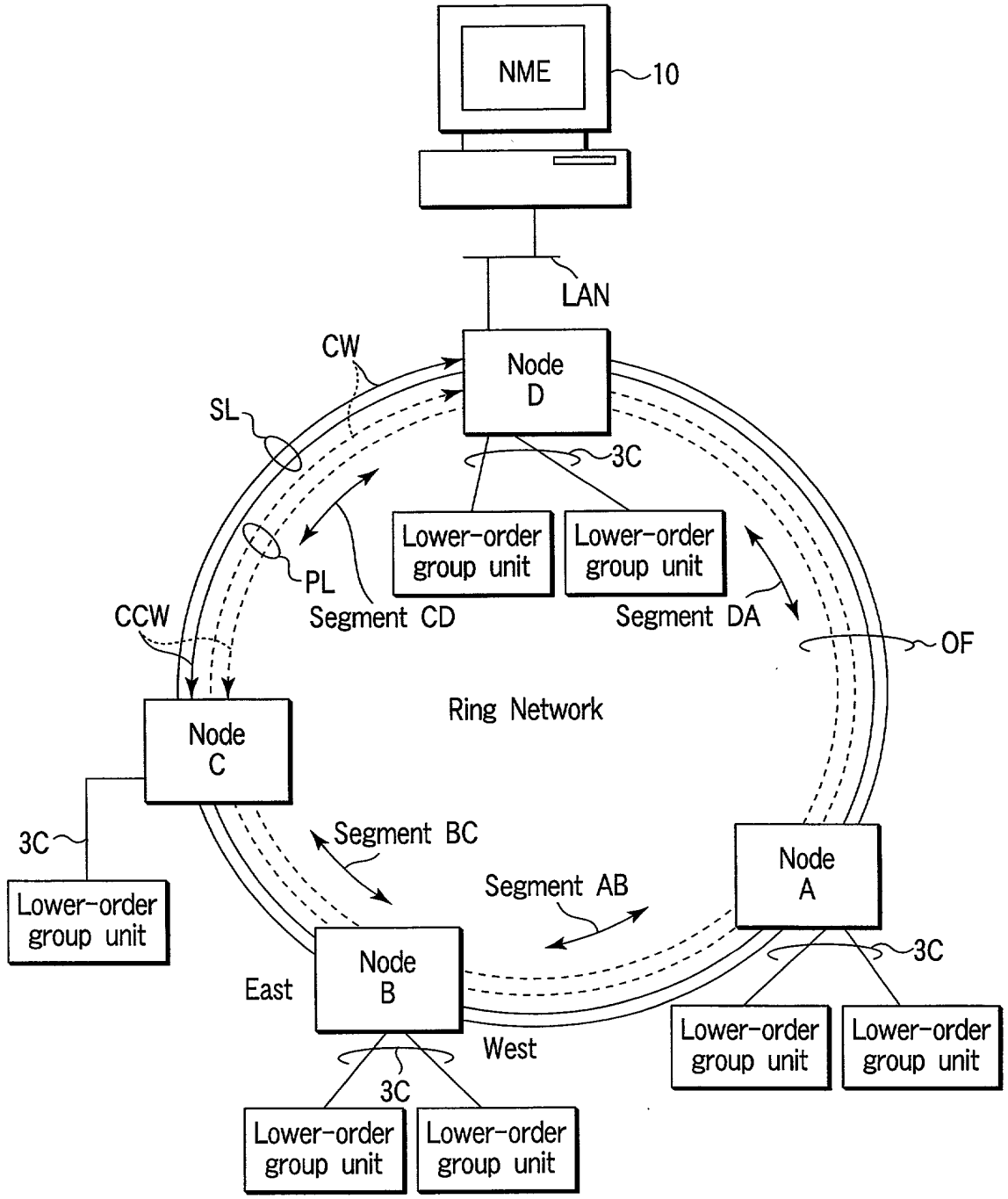


FIG. 1

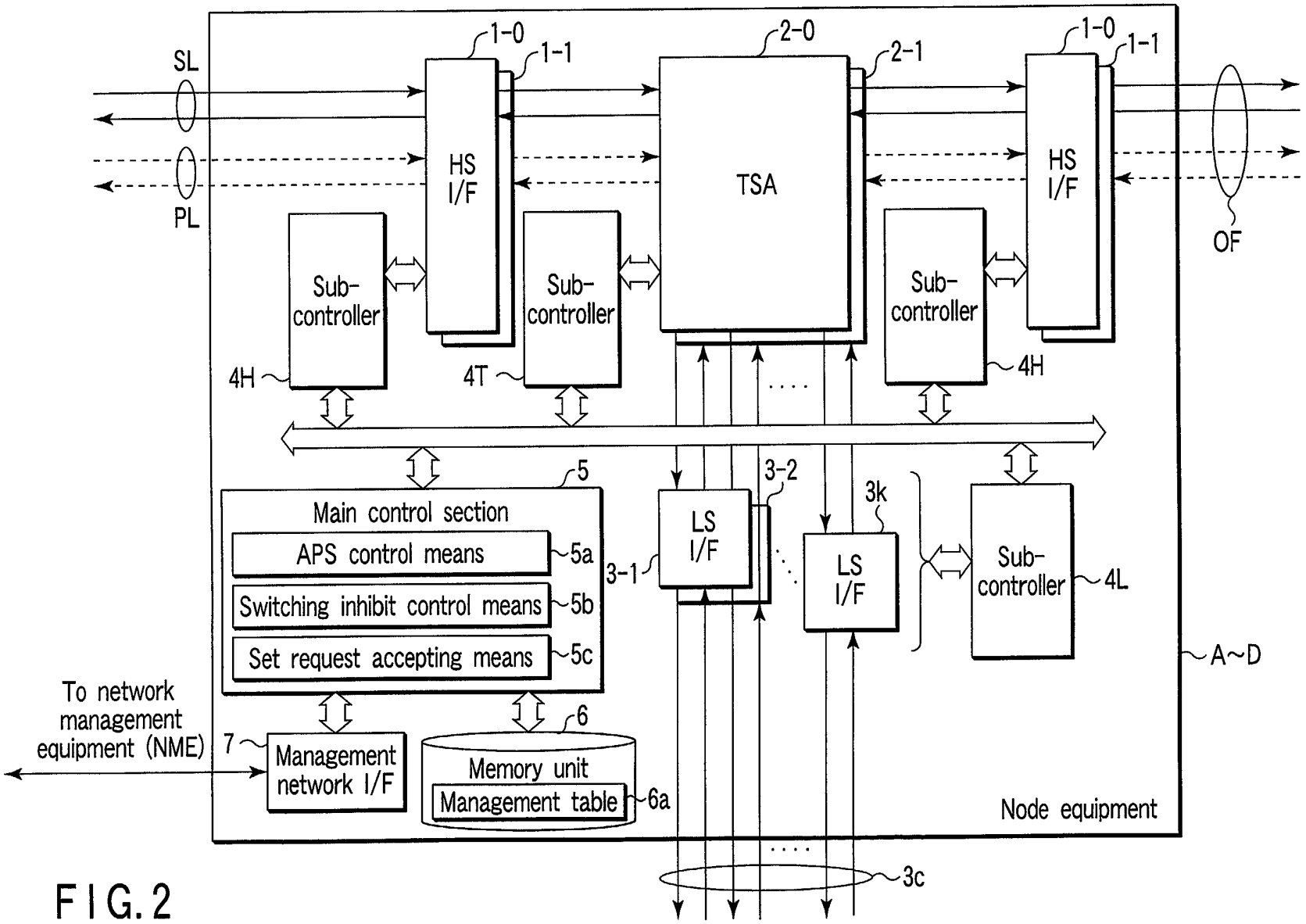

SL
PL
1-0
1-1
HS I/F
2-0
2-1
TSA
1-0
1-1
HS I/F
OF
Sub-controller
4H
Sub-controller
4T
Sub-controller
4H
5
Main control section
APS control means
5a
Switching inhibit control means
5b
Set request accepting means
5c
3-1
LS I/F
3-2
3k
LS I/F
Sub-controller
4L
A~D
To network management equipment (NME)
7
Management network I/F
6
Memory unit
Management table
6a
Node equipment
3c

FIG. 2

	Node	D				C				B				A			
	West/East	W		E		W		E		W		E		W		E	
	Span/Ring	S	R	S	R	S	R	S	R	S	R	S	R	S	R	S	R
Timeslot	TS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	•								•								
	•								•								
	•								•								
	TS64	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIG. 3

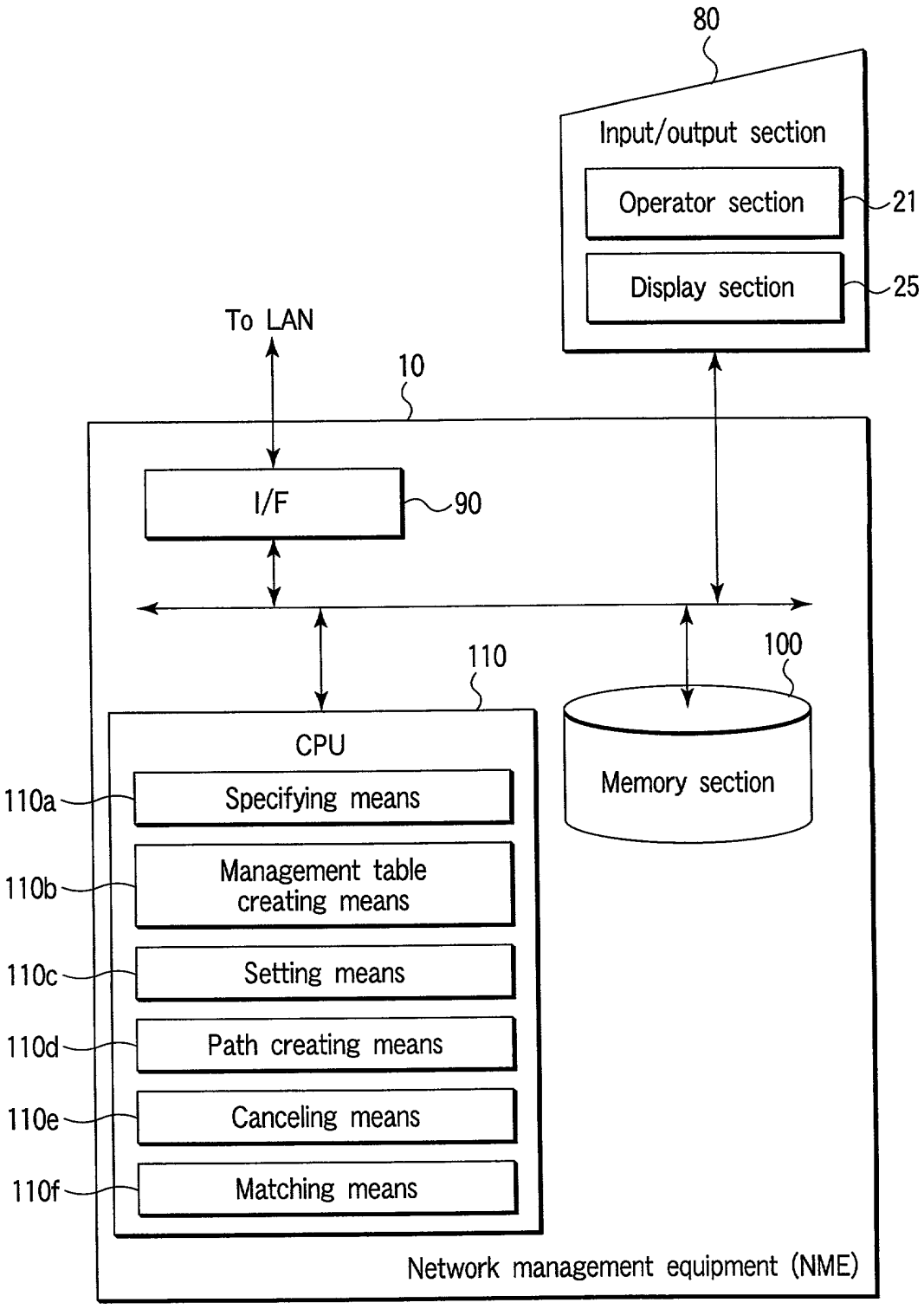

80
Input/output section
Operator section
21
Display section
25
To LAN
10
I/F
90
110
100
CPU
Memory section
110a
Specifying means
110b
Management table creating means
110c
Setting means
110d
Path creating means
110e
Canceling means
110f
Matching means
Network management equipment (NME)

FIG. 4

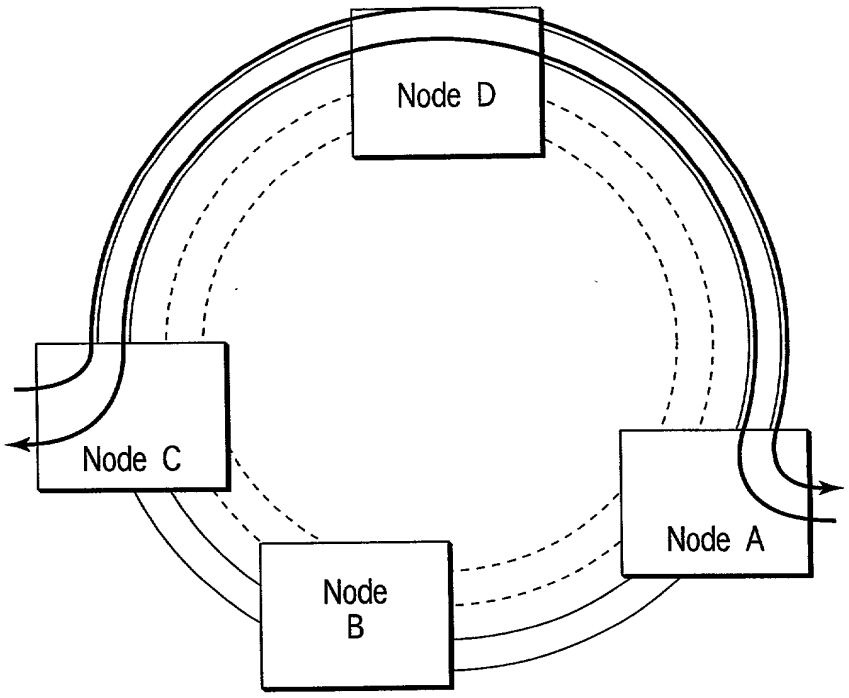


FIG. 5

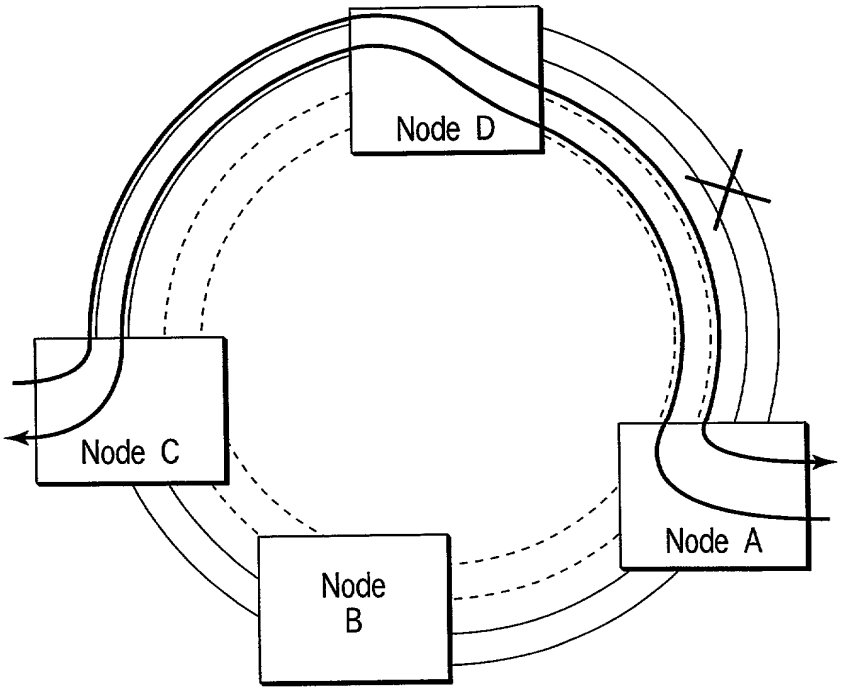


FIG. 6

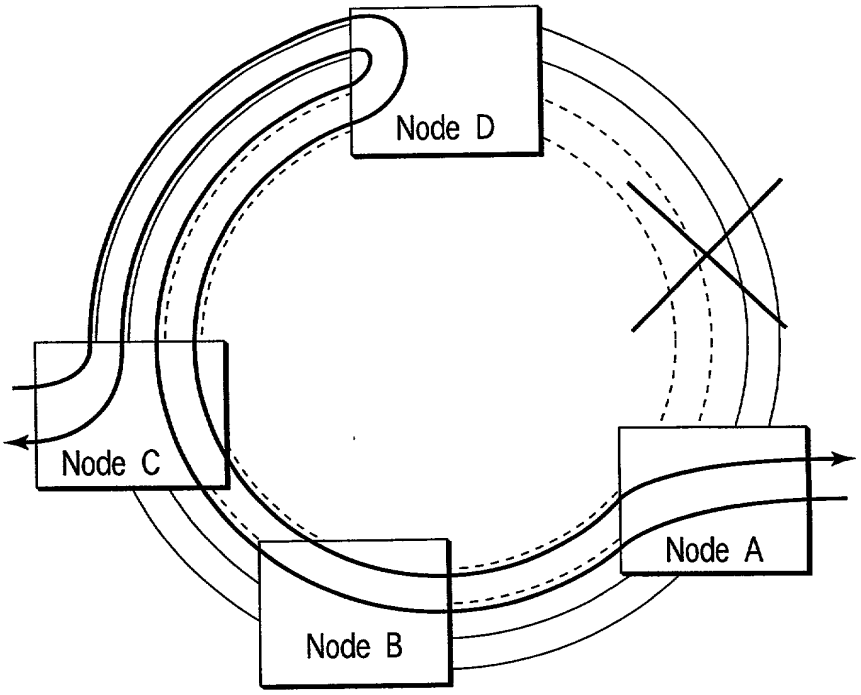


FIG. 7

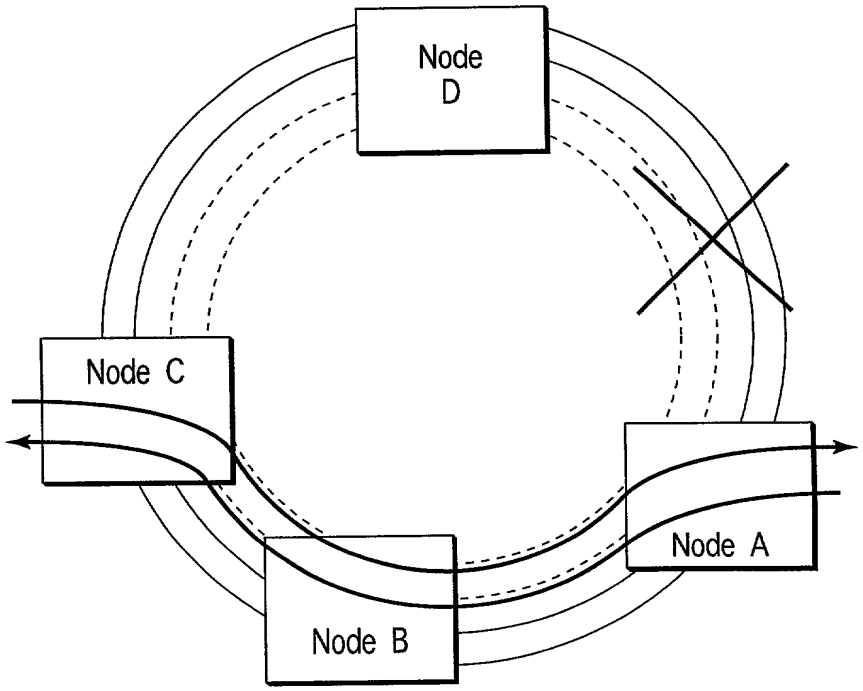


FIG. 8

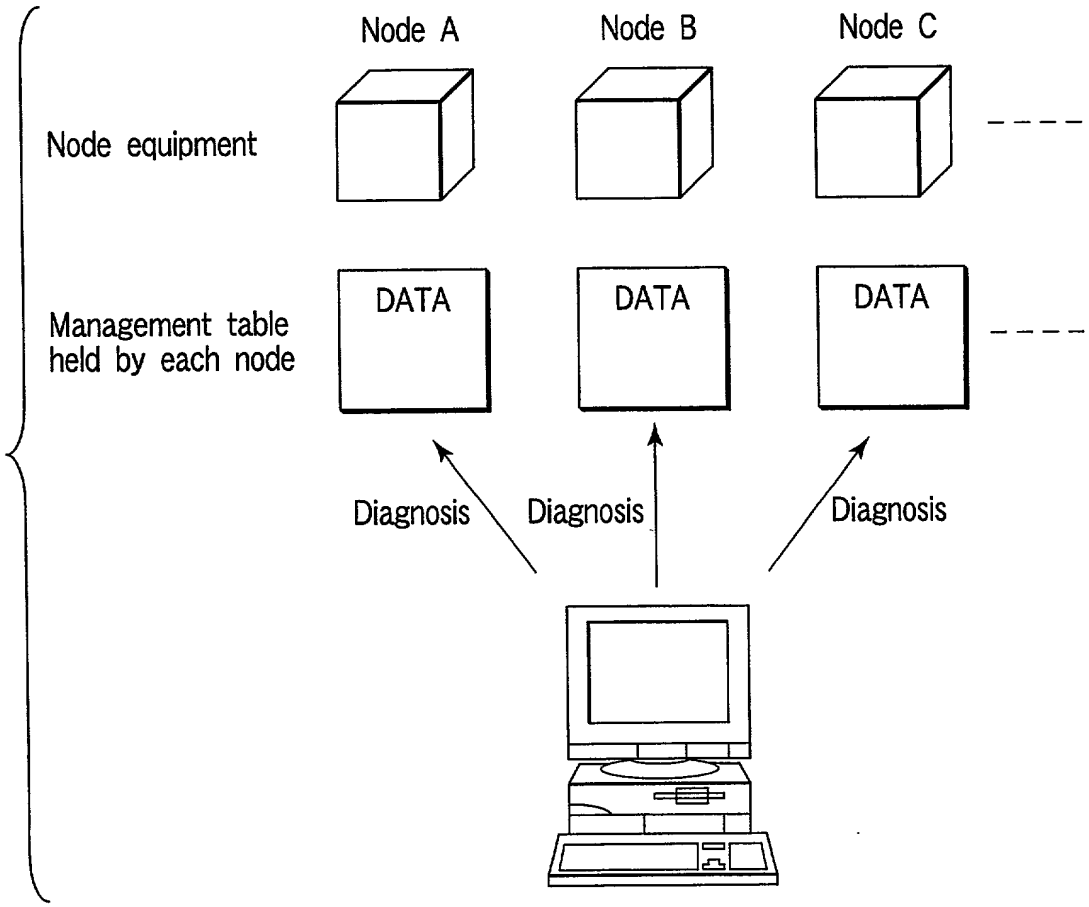

Node A
Node B
Node C
Node equipment
Management table held by each node
DATA
DATA
DATA
Diagnosis
Diagnosis
Diagnosis

FIG. 9

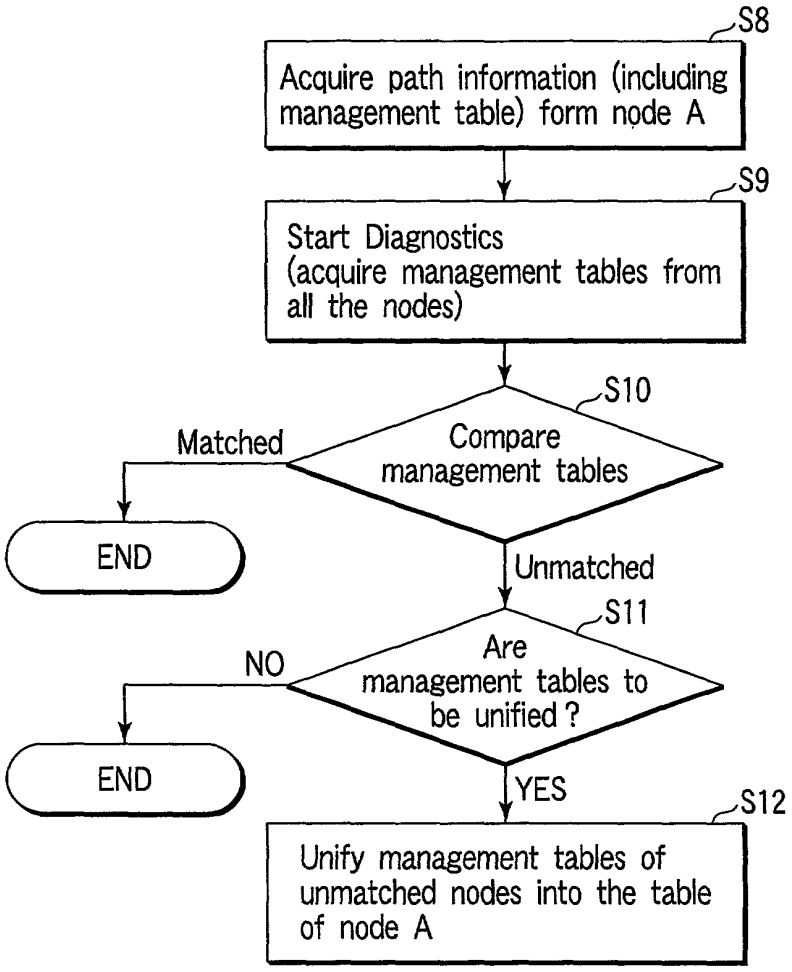


FIG. 10

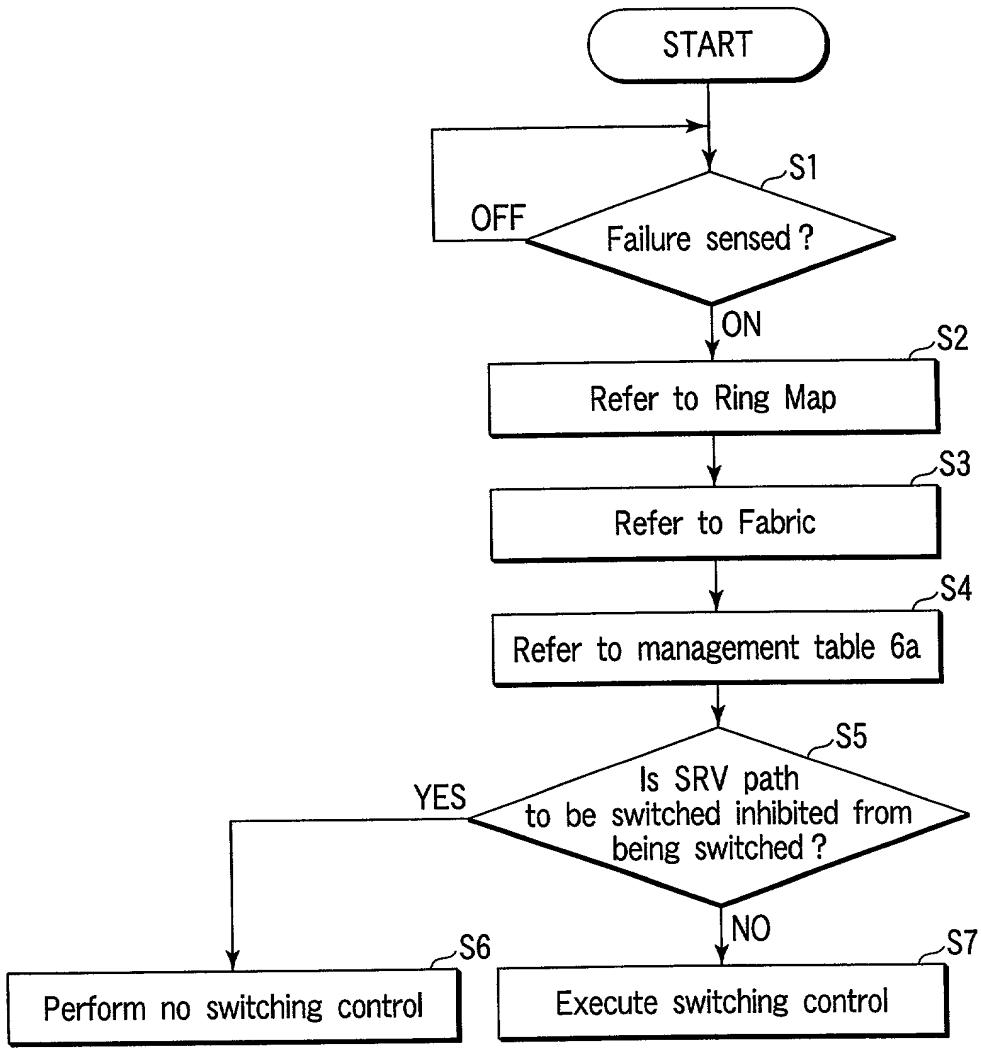

START
S1
OFF
Failure sensed ?
ON
S2
Refer to Ring Map
S3
Refer to Fabric
S4
Refer to management table 6a
S5
YES
Is SRV path to be switched inhibited from being switched ?
NO
S6
Perform no switching control
S7
Execute switching control

FIG. 11

	Node	D				C				B				A			
	West/East	W		E		W		E		W		E		W		E	
	Span/Ring	S	R	S	R	S	R	S	R	S	R	S	R	S	R	S	R
Timeslot	TS1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	TS2	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	TS3	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	TS4	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	•							•									
	•							•									
	•							•									
	TS64	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0

FIG. 12

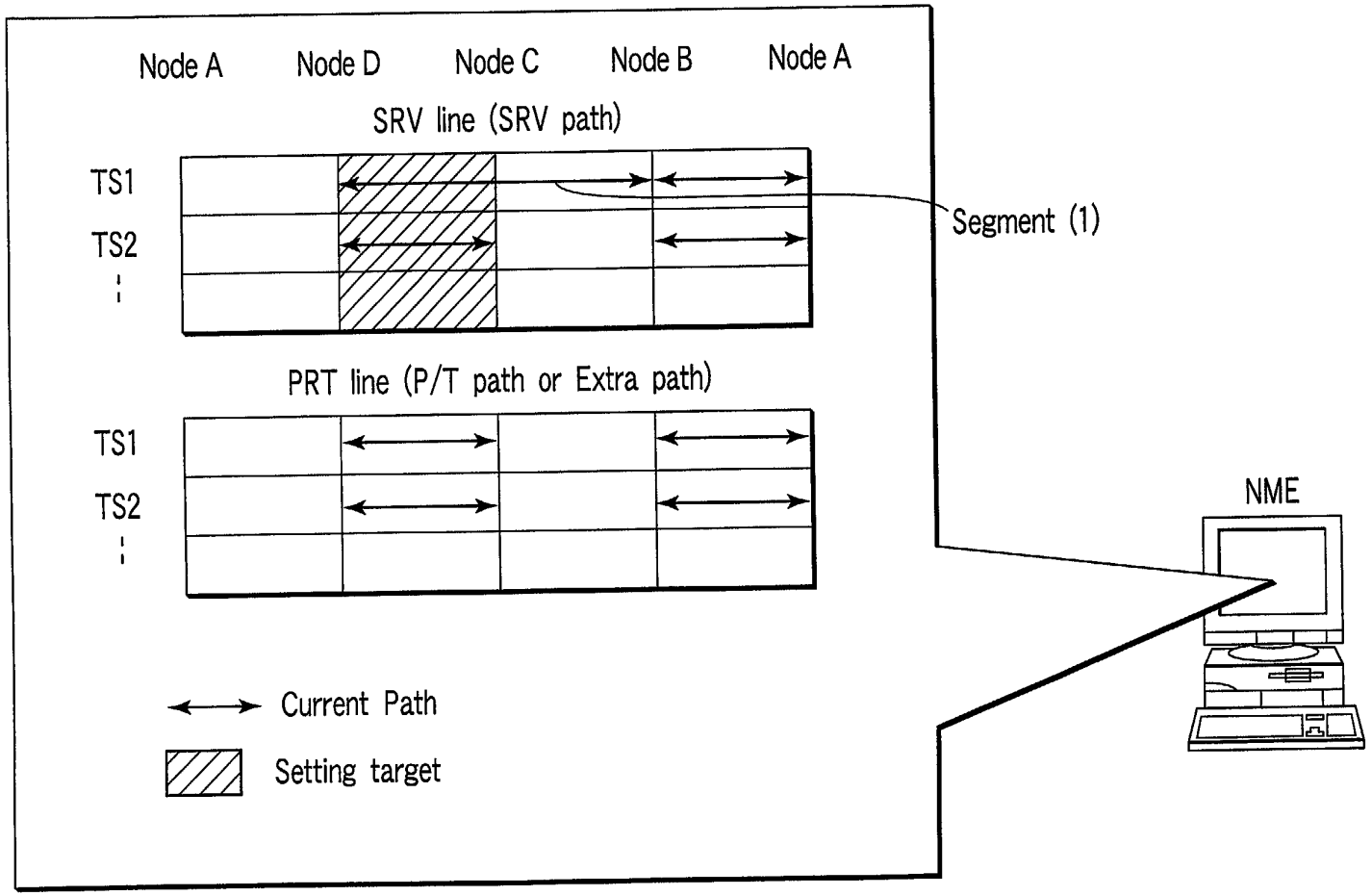

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
Segment (1)
PRT line (P/T path or Extra path)
TS1
TS2
NME
Current Path
Setting target

FIG. 13

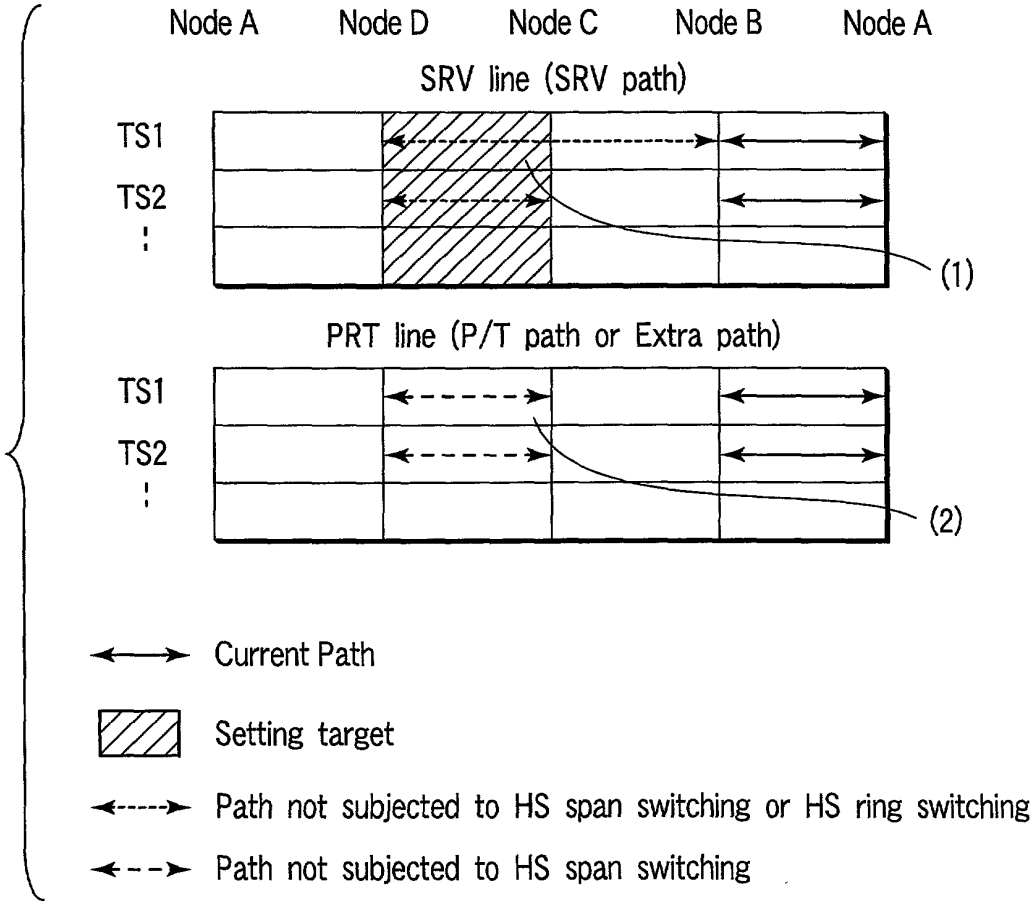
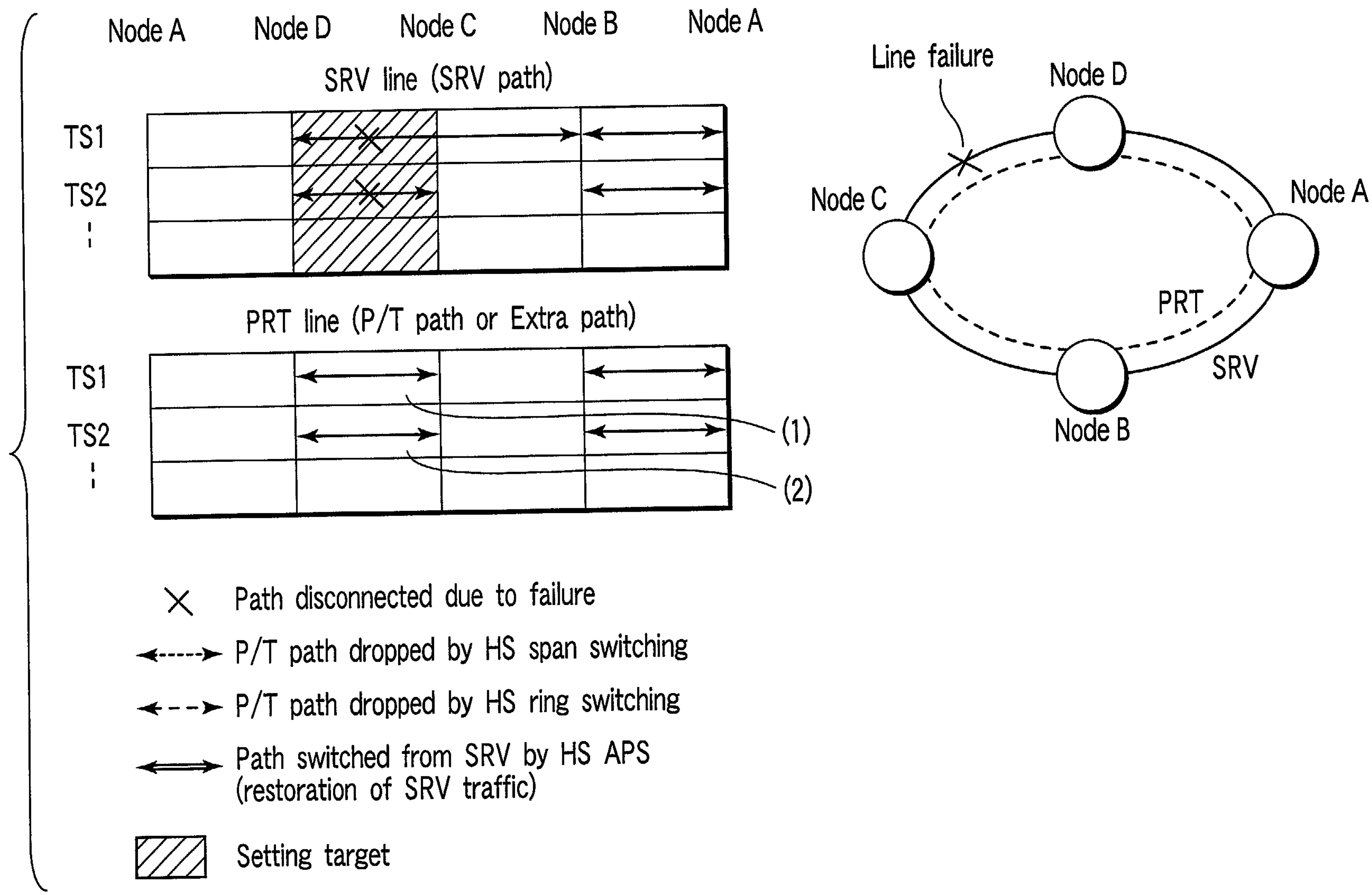


FIG. 14


Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Line failure
Node D
Node C
Node A
PRT
SRV
Node B
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS (restoration of SRV traffic)
Setting target

F I G. 15

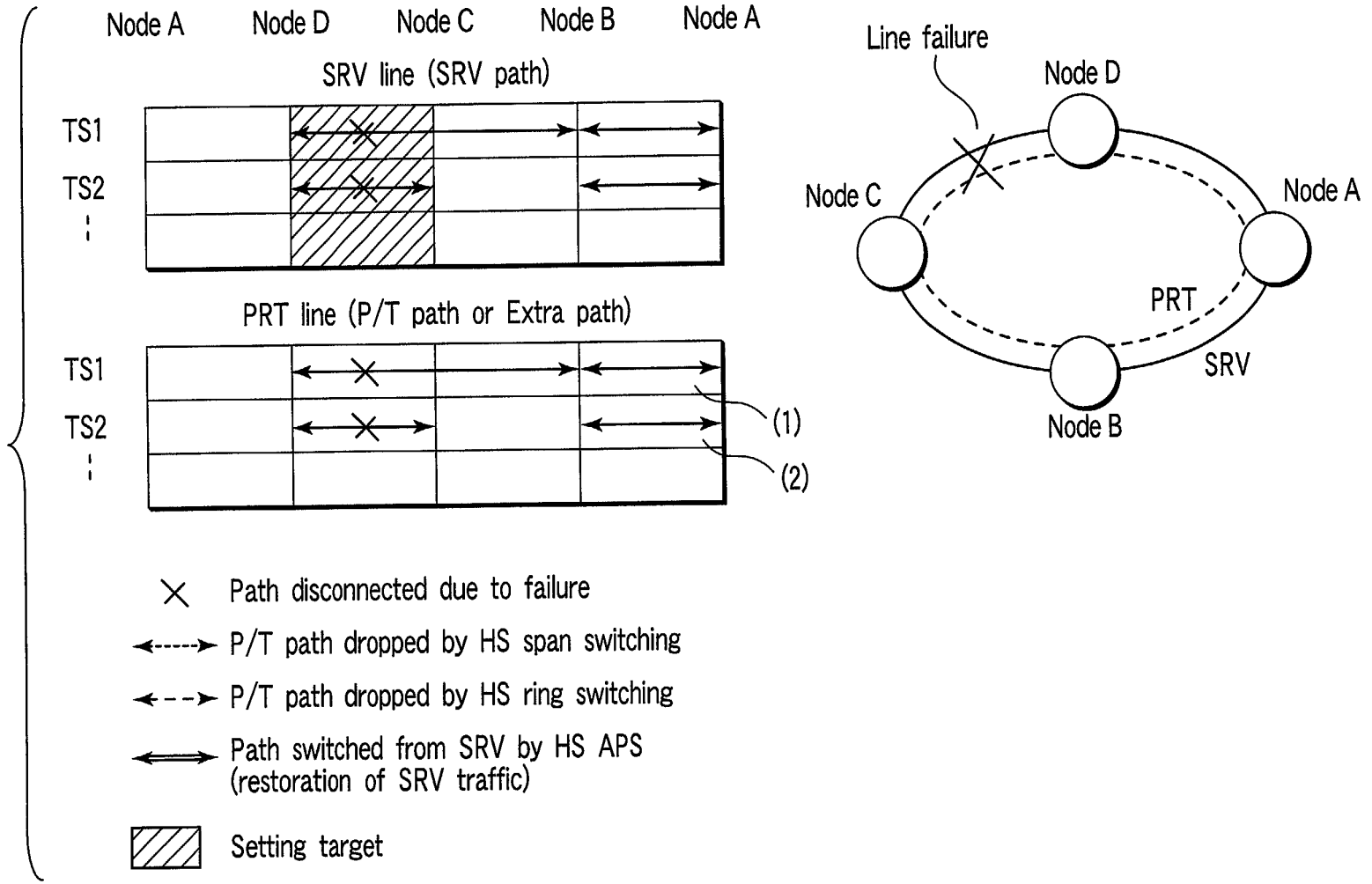

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 16

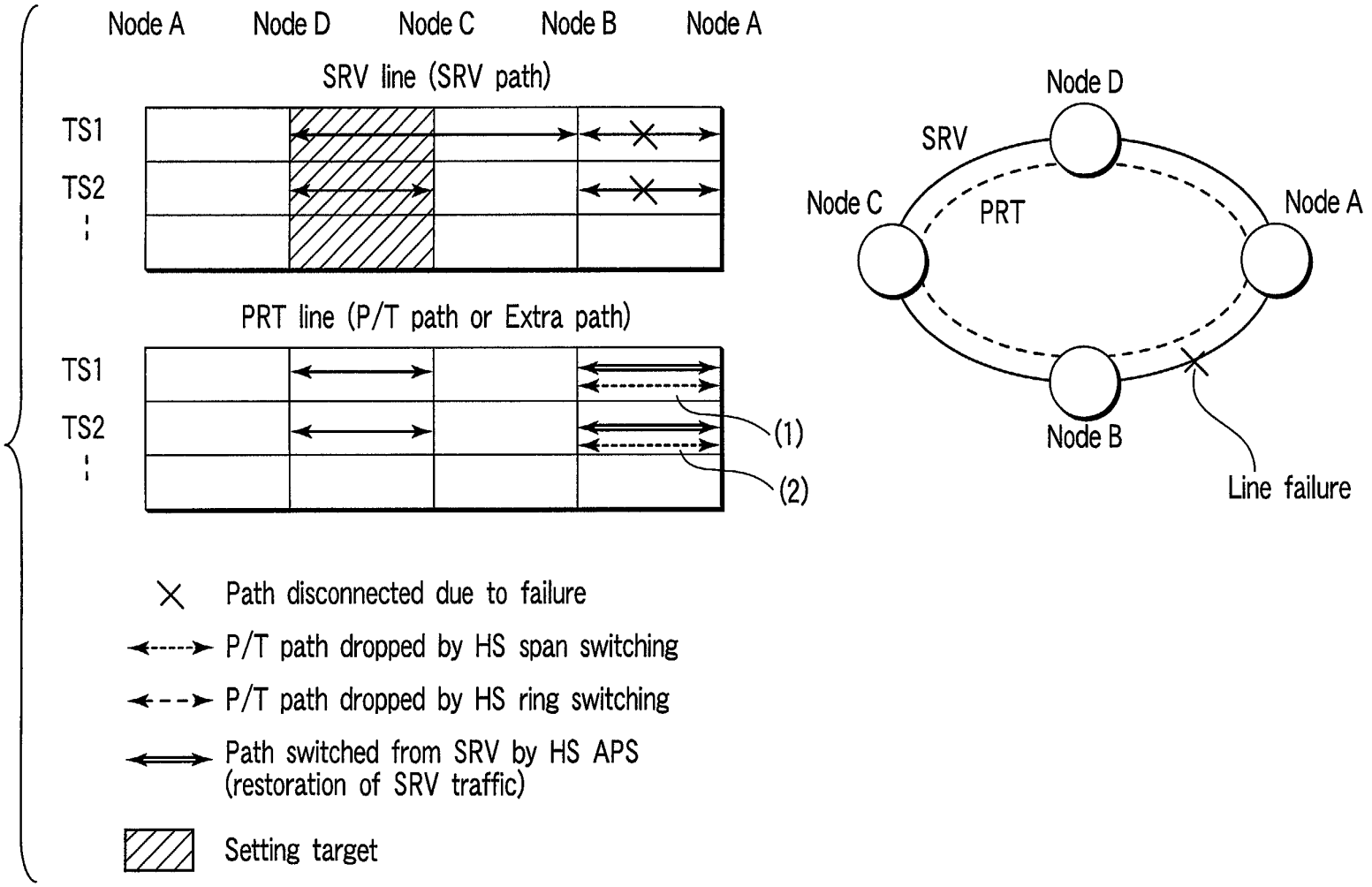

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Node D
SRV
Node C
PRT
Node A
Node B
Line failure

FIG. 17

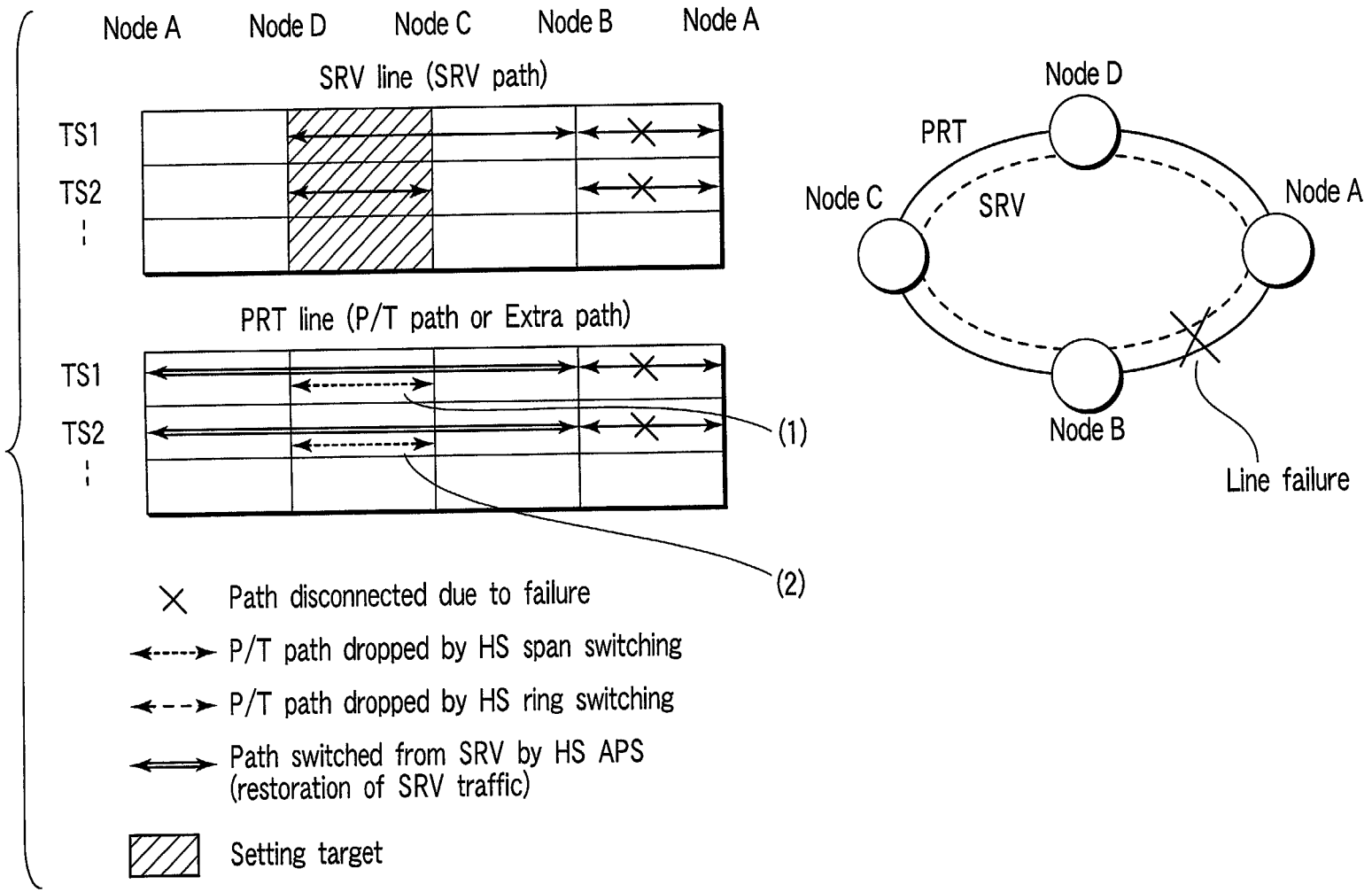

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Node D
PRT
Node C
SRV
Node A
Node B
Line failure

FIG. 18

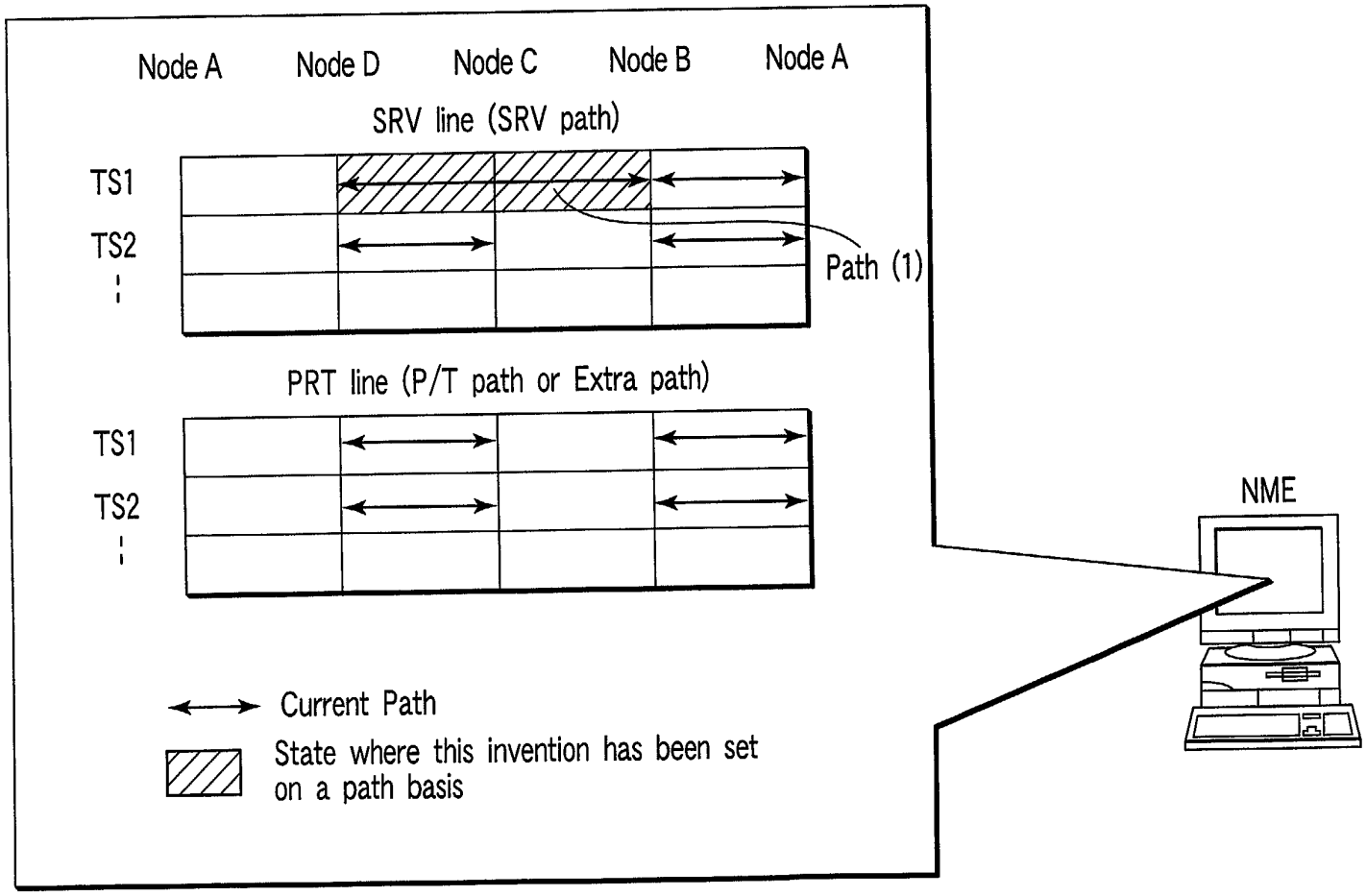

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
Path (1)
PRT line (P/T path or Extra path)
TS1
TS2
NME
Current Path
State where this invention has been set on a path basis

FIG. 19

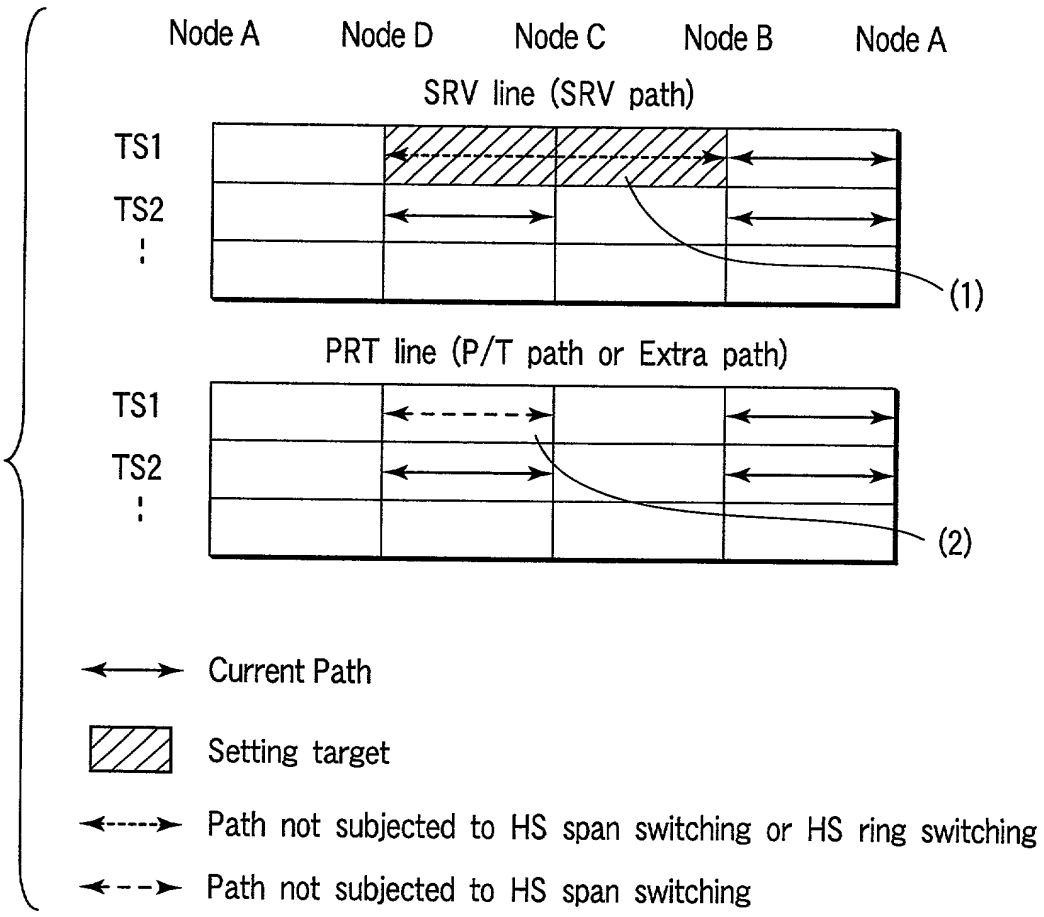

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
(1)
PRT line (P/T path or Extra path)
TS1
TS2
(2)
Current Path
Setting target
Path not subjected to HS span switching or HS ring switching
Path not subjected to HS span switching

FIG. 20

	Node	D				C				B				A			
	West/East	W		E		W		E		W		E		W		E	
	Span/Ring	S	R	S	R	S	R	S	R	S	R	S	R	S	R	S	R
Timeslot	TS1	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	TS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	•								•								
	•								•								
	•								•								
	TS64	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIG. 21

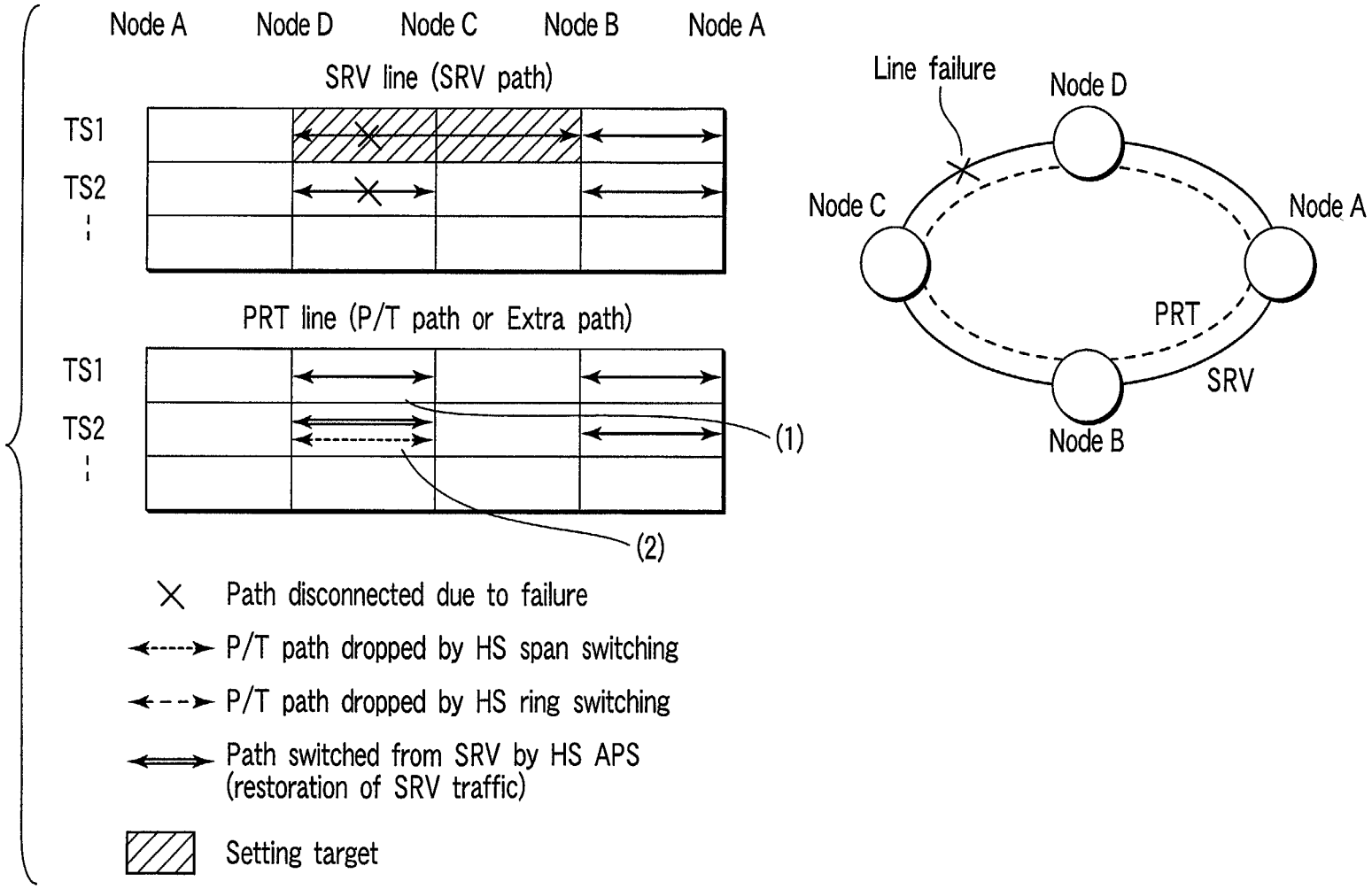

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 22

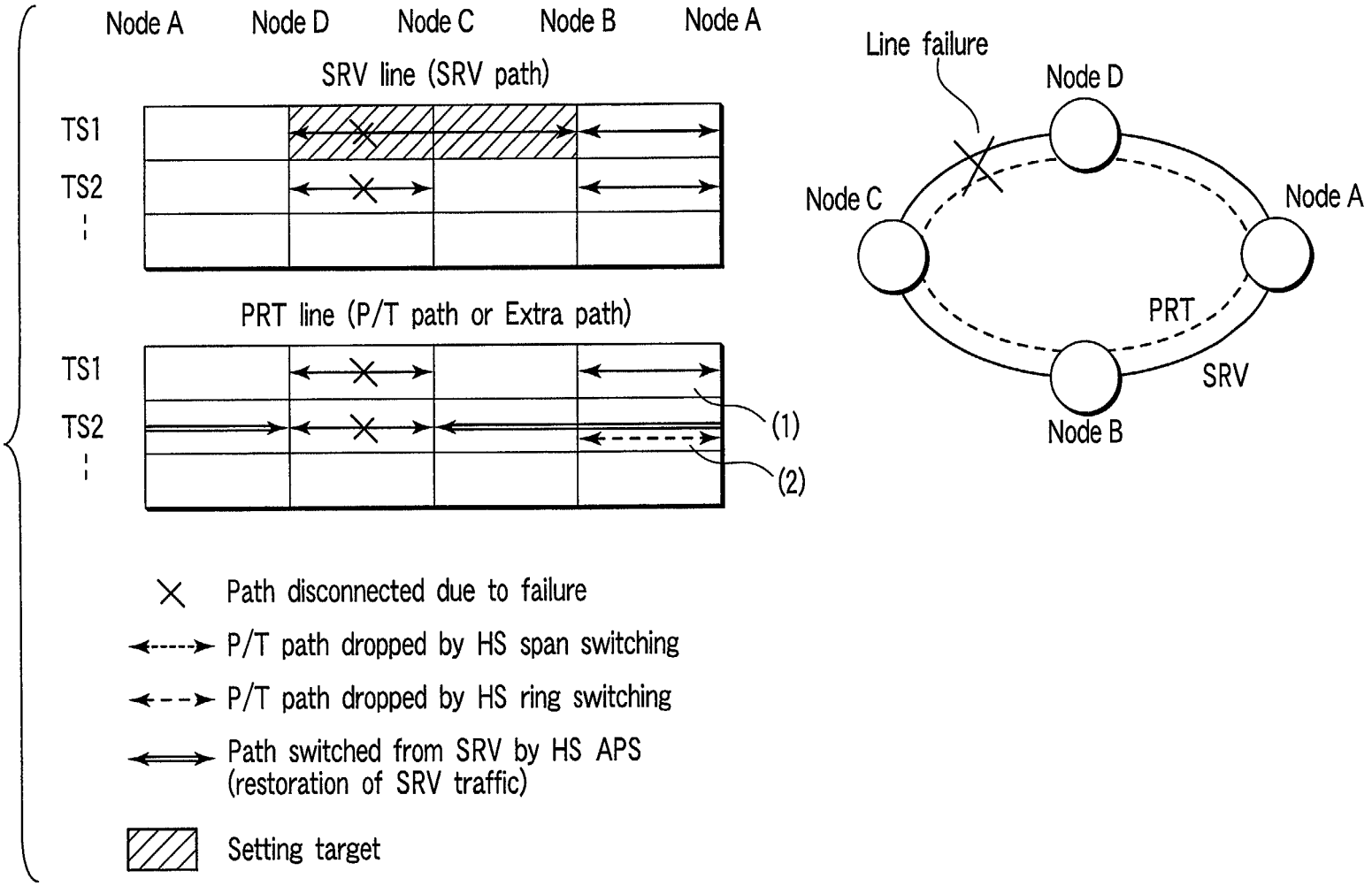

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 23

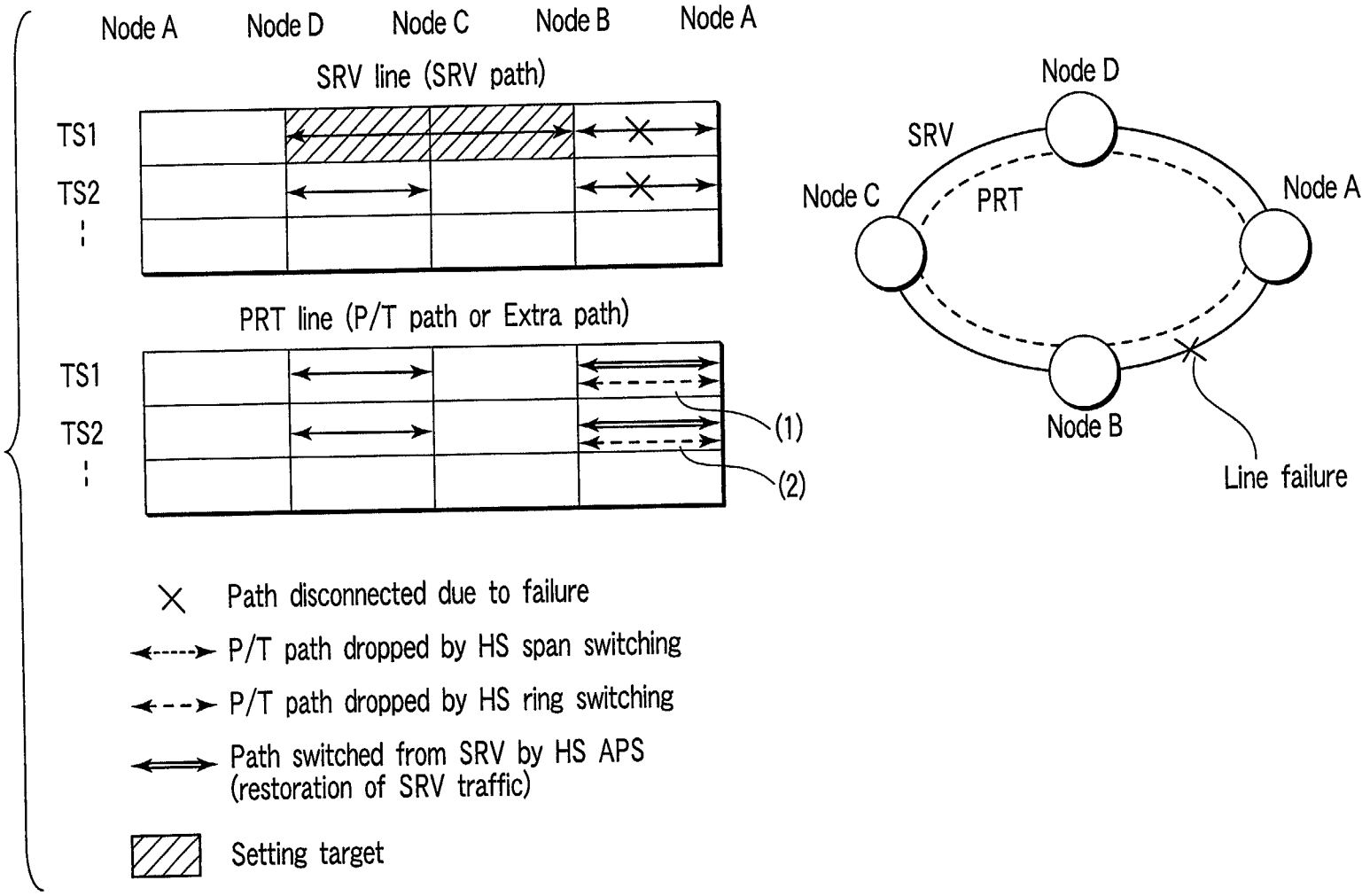

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Node D
SRV
Node C
PRT
Node A
Node B
Line failure

FIG. 24

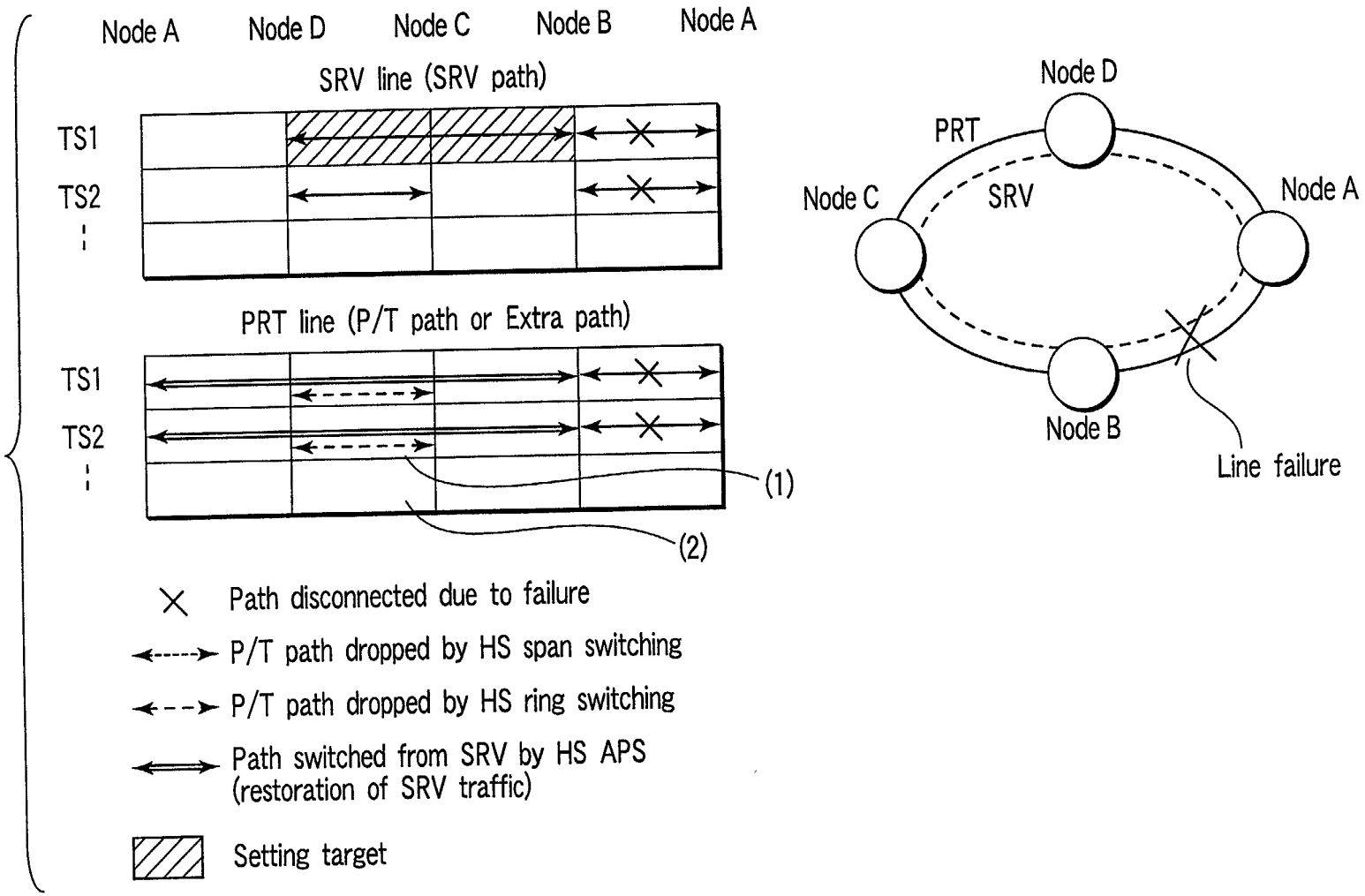

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Node D
PRT
Node C
SRV
Node A
Node B
Line failure

FIG. 25

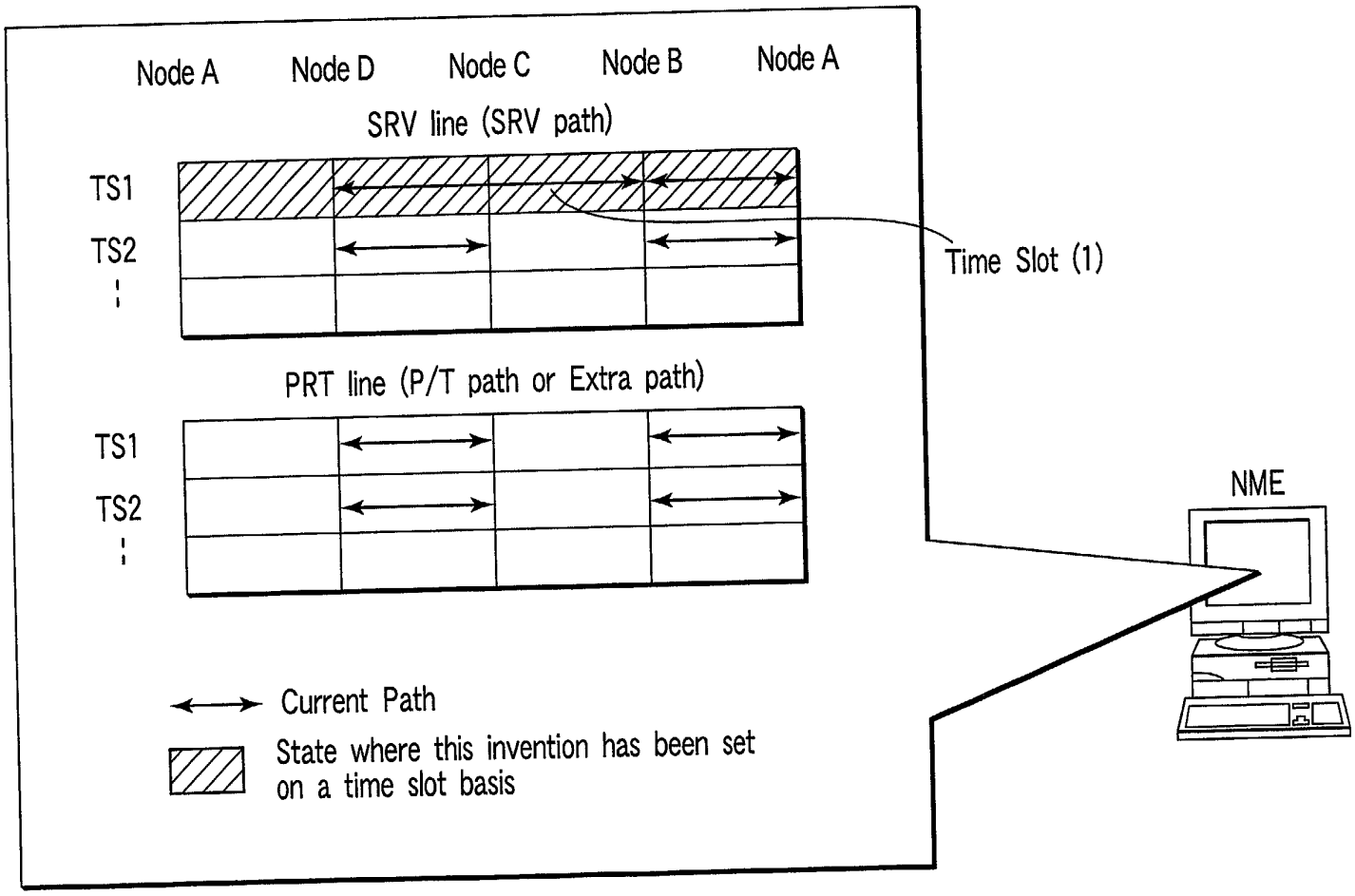

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
Time Slot (1)
PRT line (P/T path or Extra path)
TS1
TS2
NME
Current Path
State where this invention has been set on a time slot basis

FIG. 26

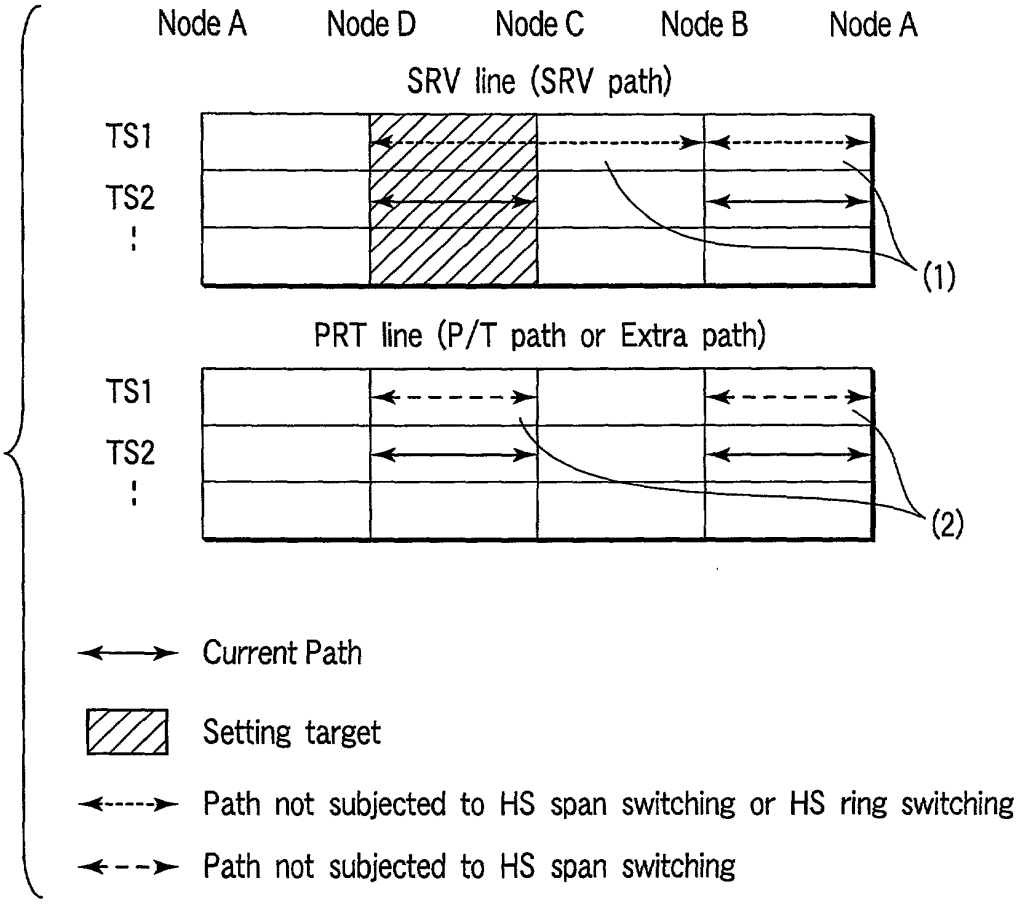


FIG. 27

	Node	D				C				B				A			
	West/East	W		E		W		E		W		E		W		E	
	Span/Ring	S	R	S	R	S	R	S	R	S	R	S	R	S	R	S	R
Timeslot	TS1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	TS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	•								•								
	•								•								
	•								•								
	TS64	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIG. 28

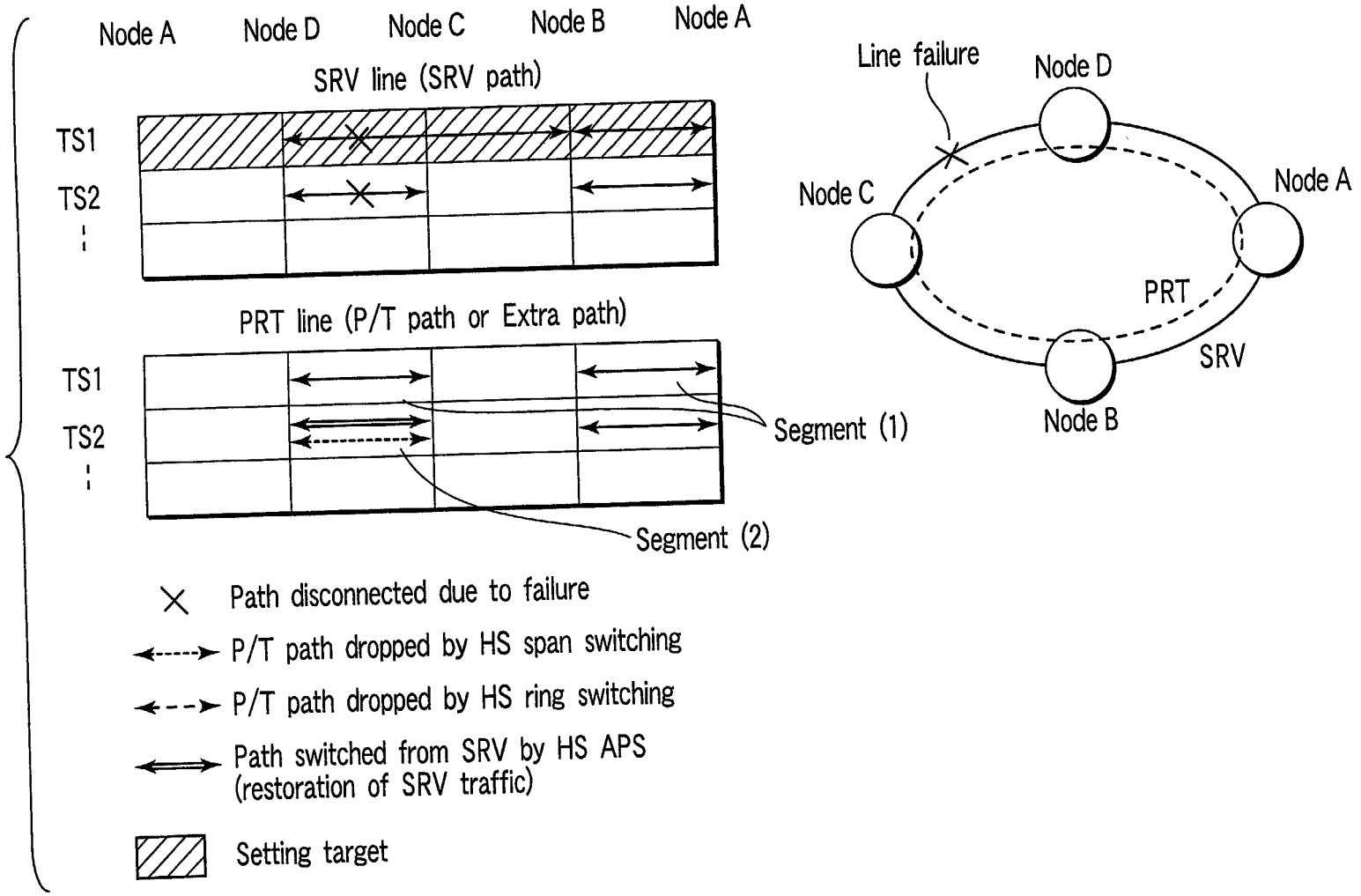

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 29

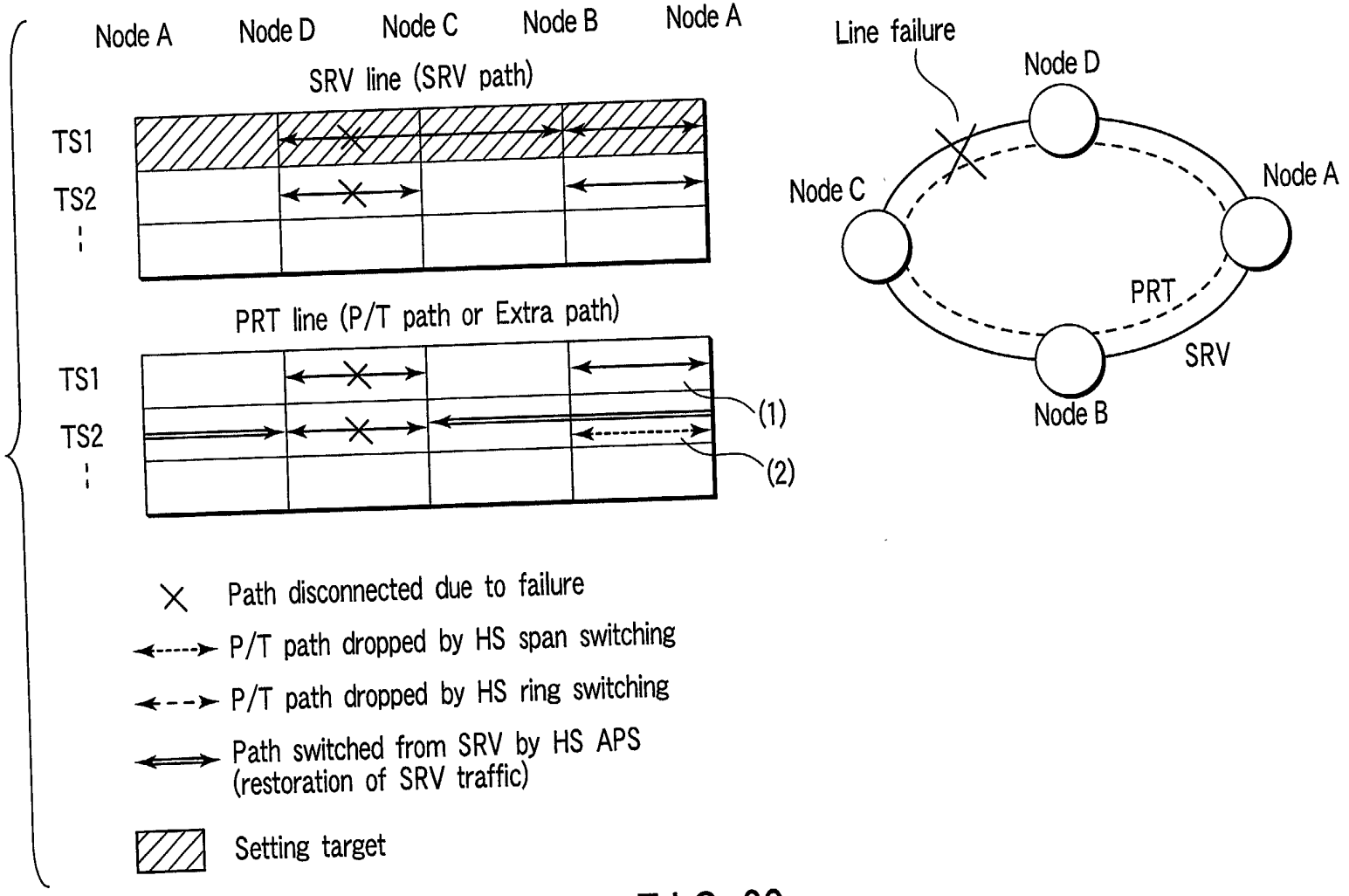

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 30

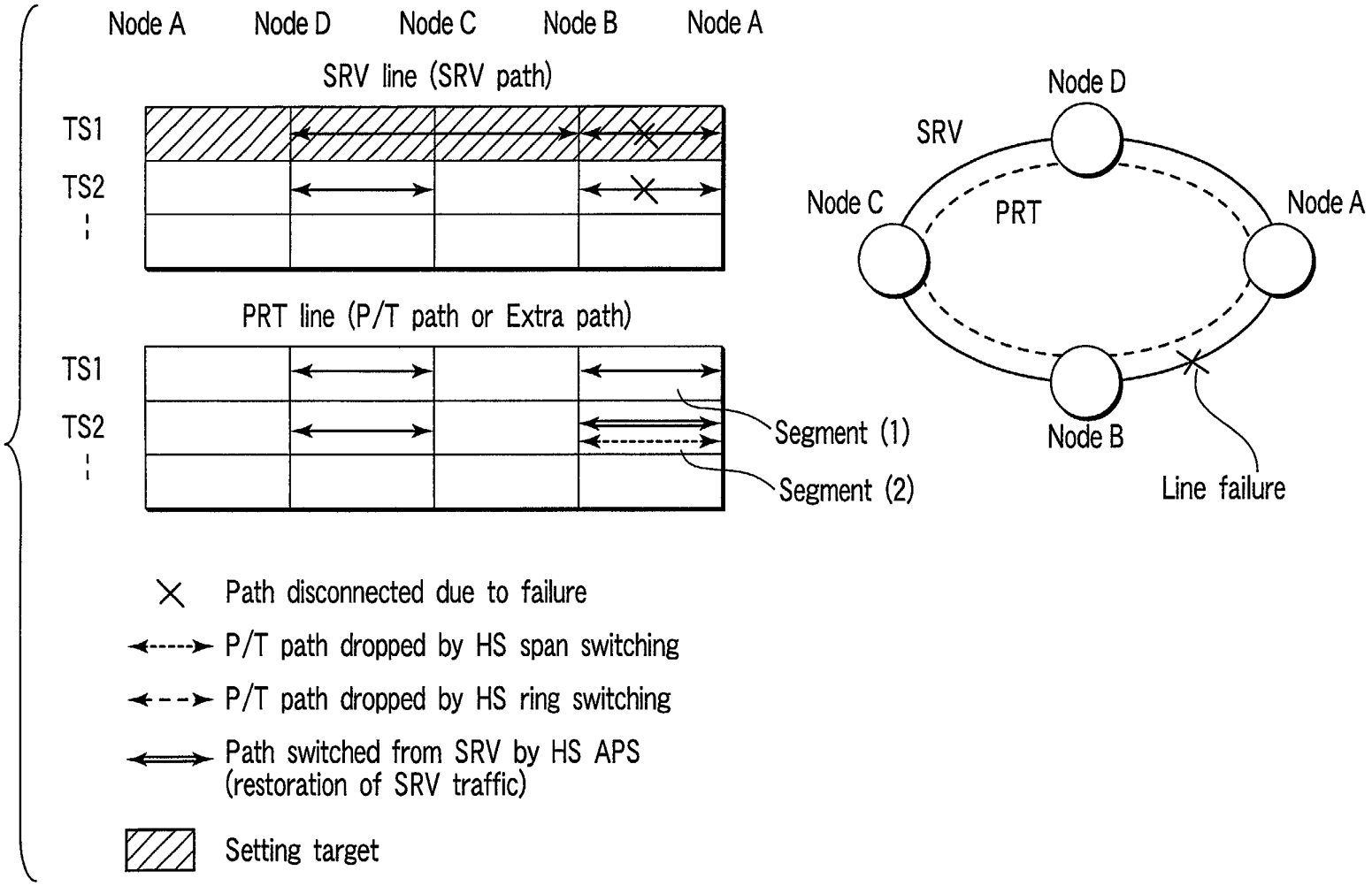

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Node D
SRV
Node C
PRT
Node A
Node B
Line failure
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target

FIG. 31

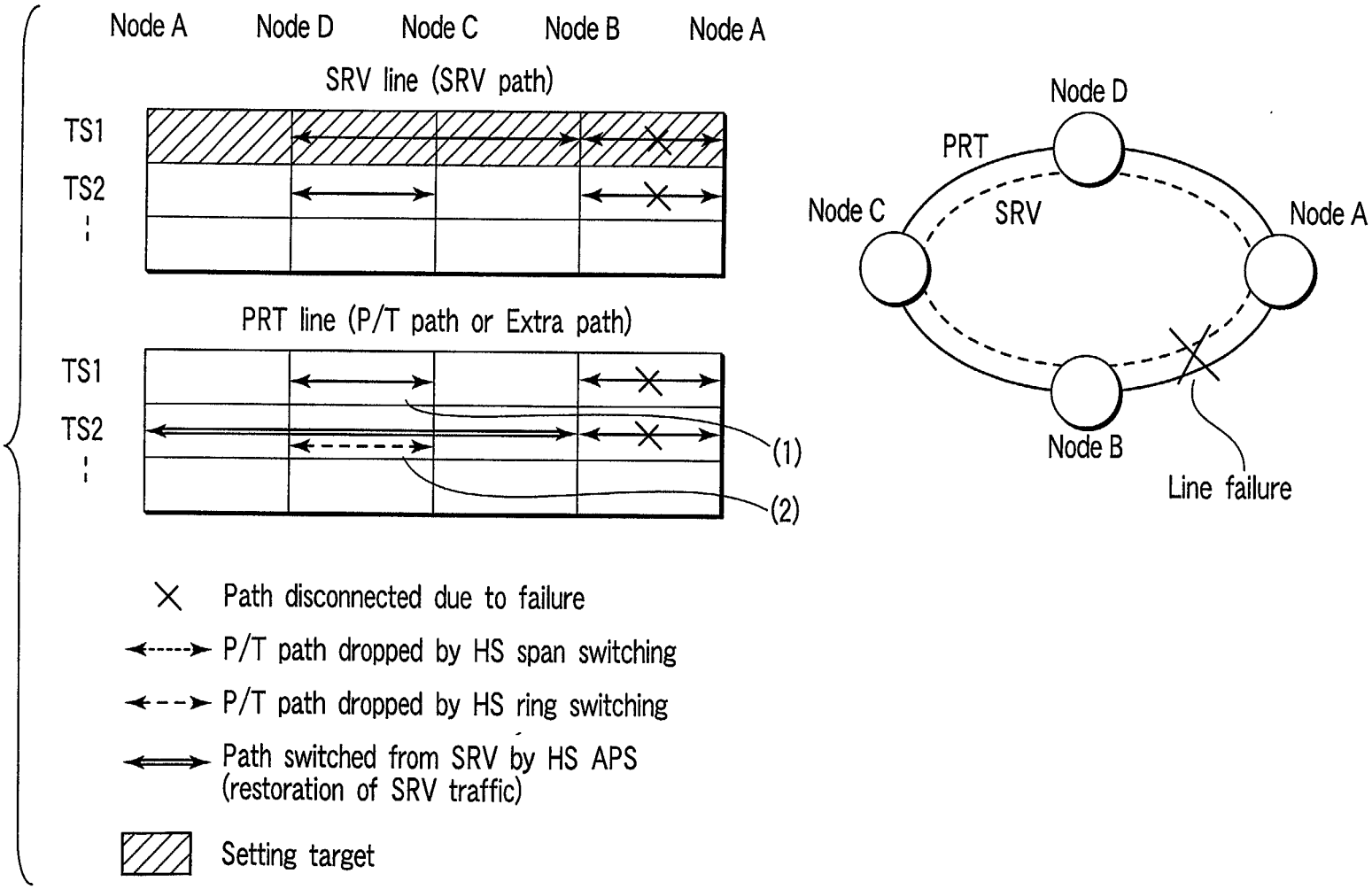

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Node D
PRT
Node C
SRV
Node A
Node B
Line failure

FIG. 32

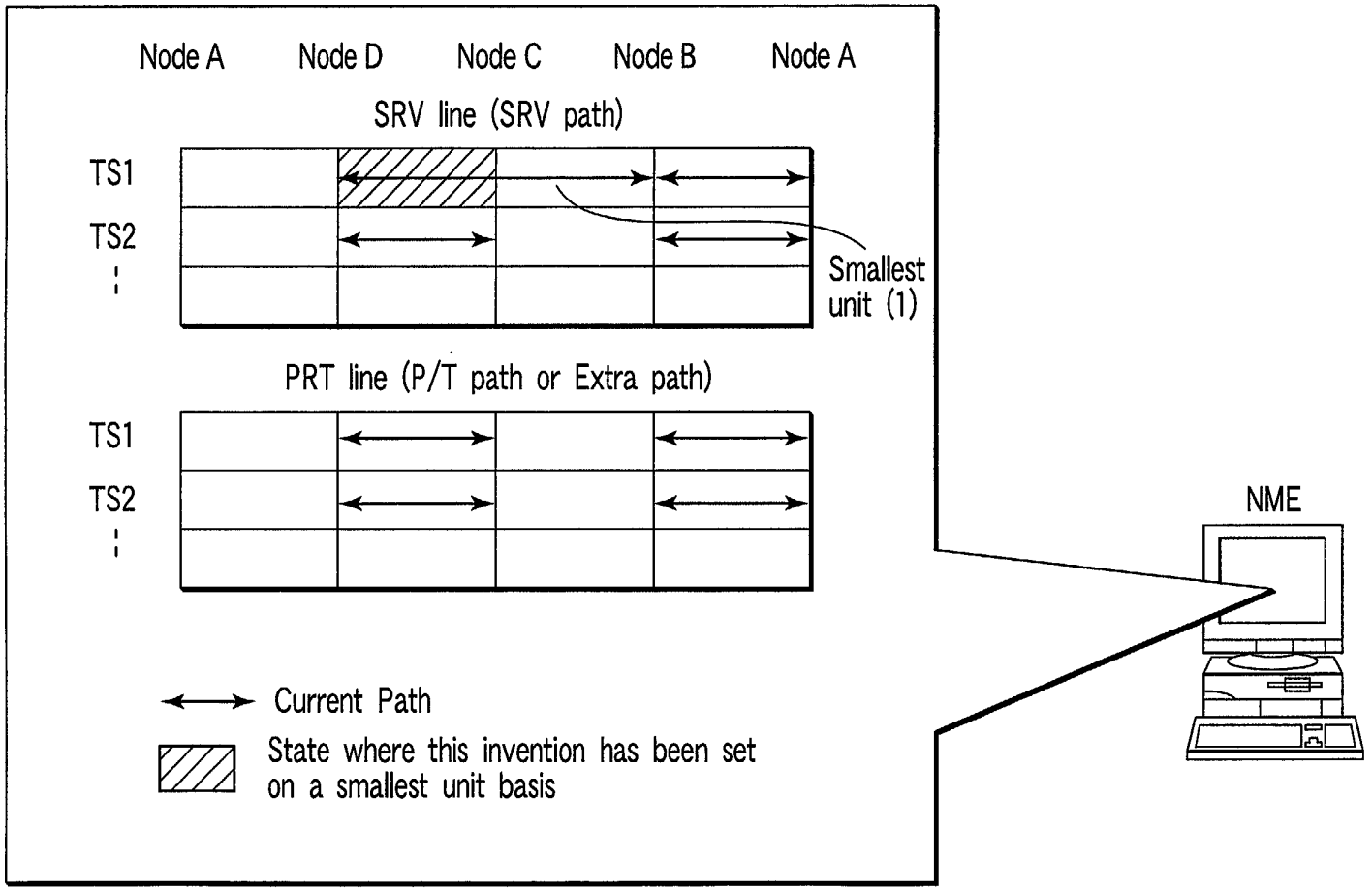

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
Smallest unit (1)
PRT line (P/T path or Extra path)
TS1
TS2
NME
Current Path
State where this invention has been set on a smallest unit basis

FIG. 33

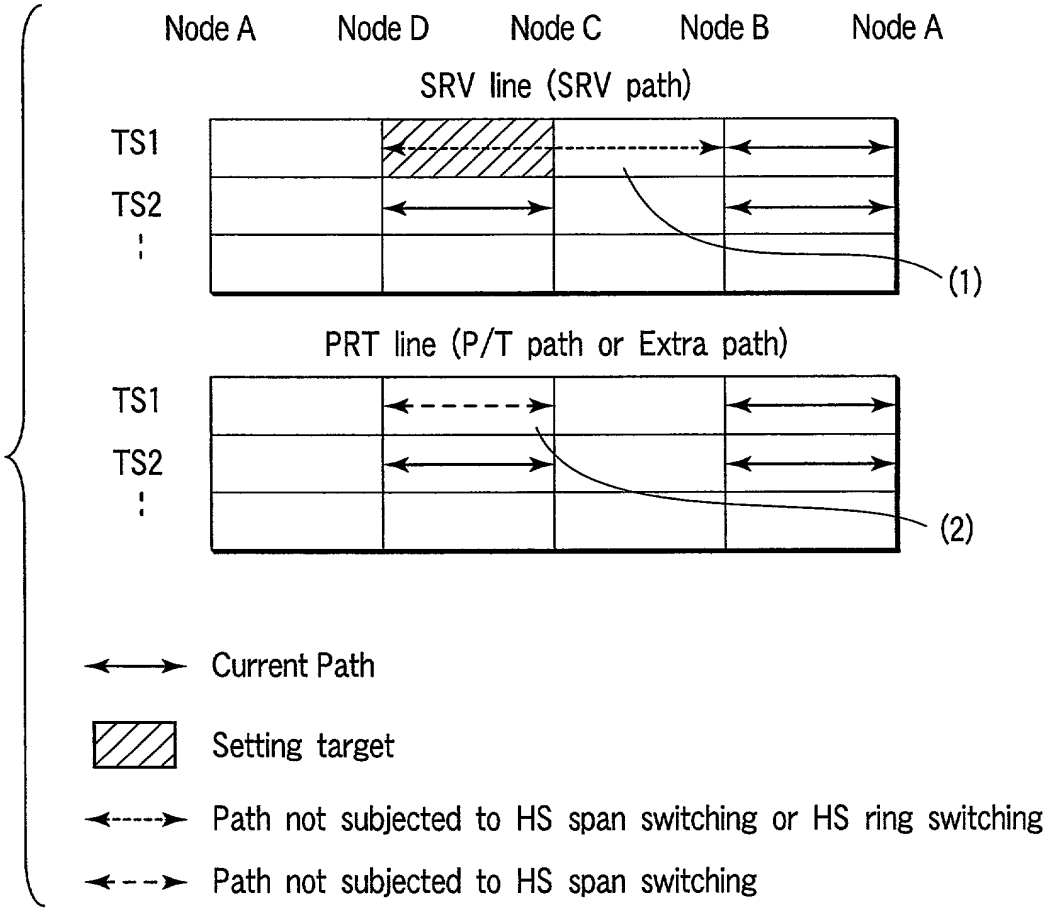

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
(1)
PRT line (P/T path or Extra path)
TS1
TS2
(2)
Current Path
Setting target
Path not subjected to HS span switching or HS ring switching
Path not subjected to HS span switching

FIG. 34

	Node	D				C				B				A			
	West/East	W		E		W		E		W		E		W		E	
	Span/Ring	S	R	S	R	S	R	S	R	S	R	S	R	S	R	S	R
Timeslot	TS1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	TS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	•								•								
	•								•								
	•								•								
	TS64	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIG. 35

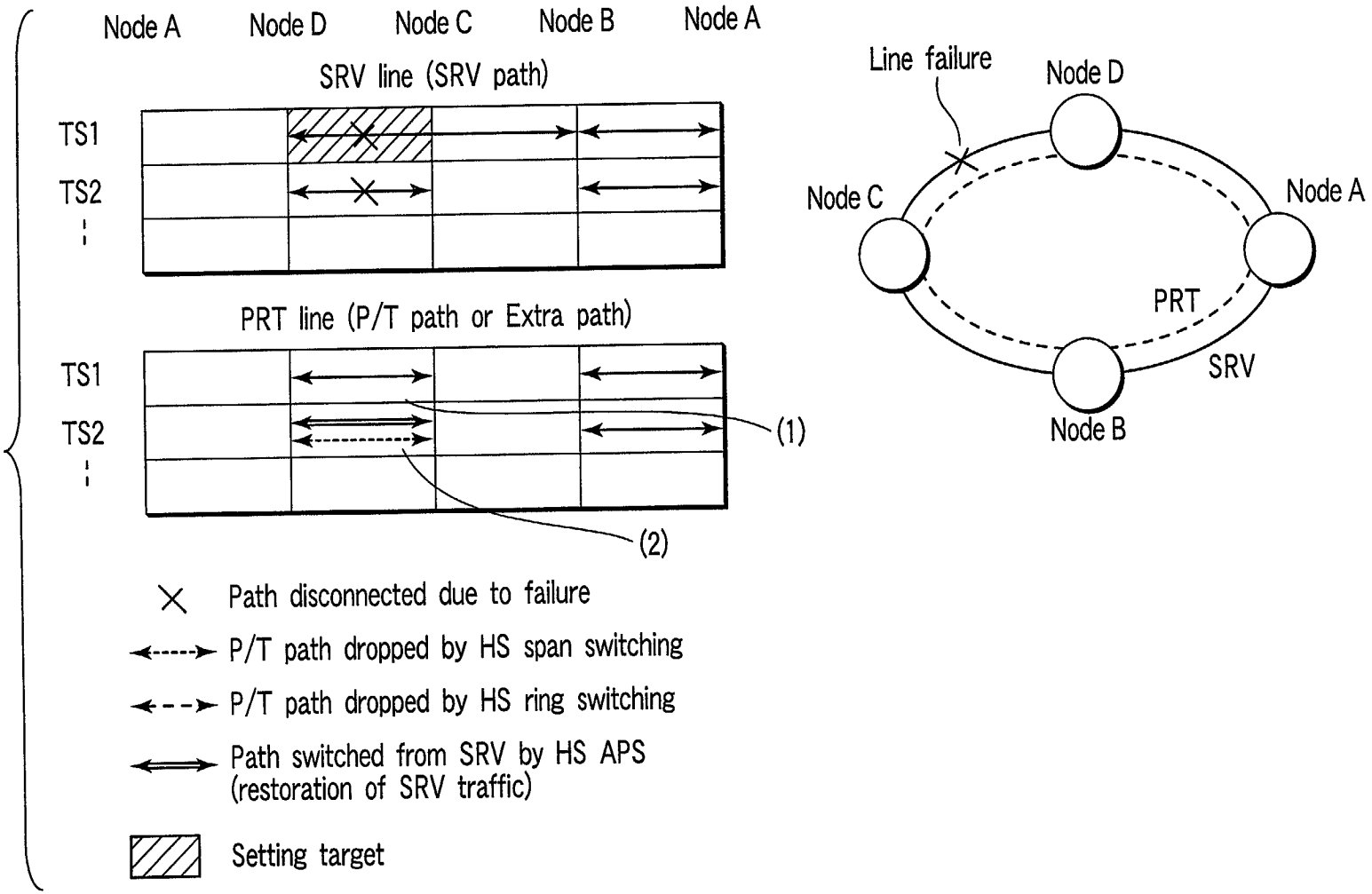

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 36

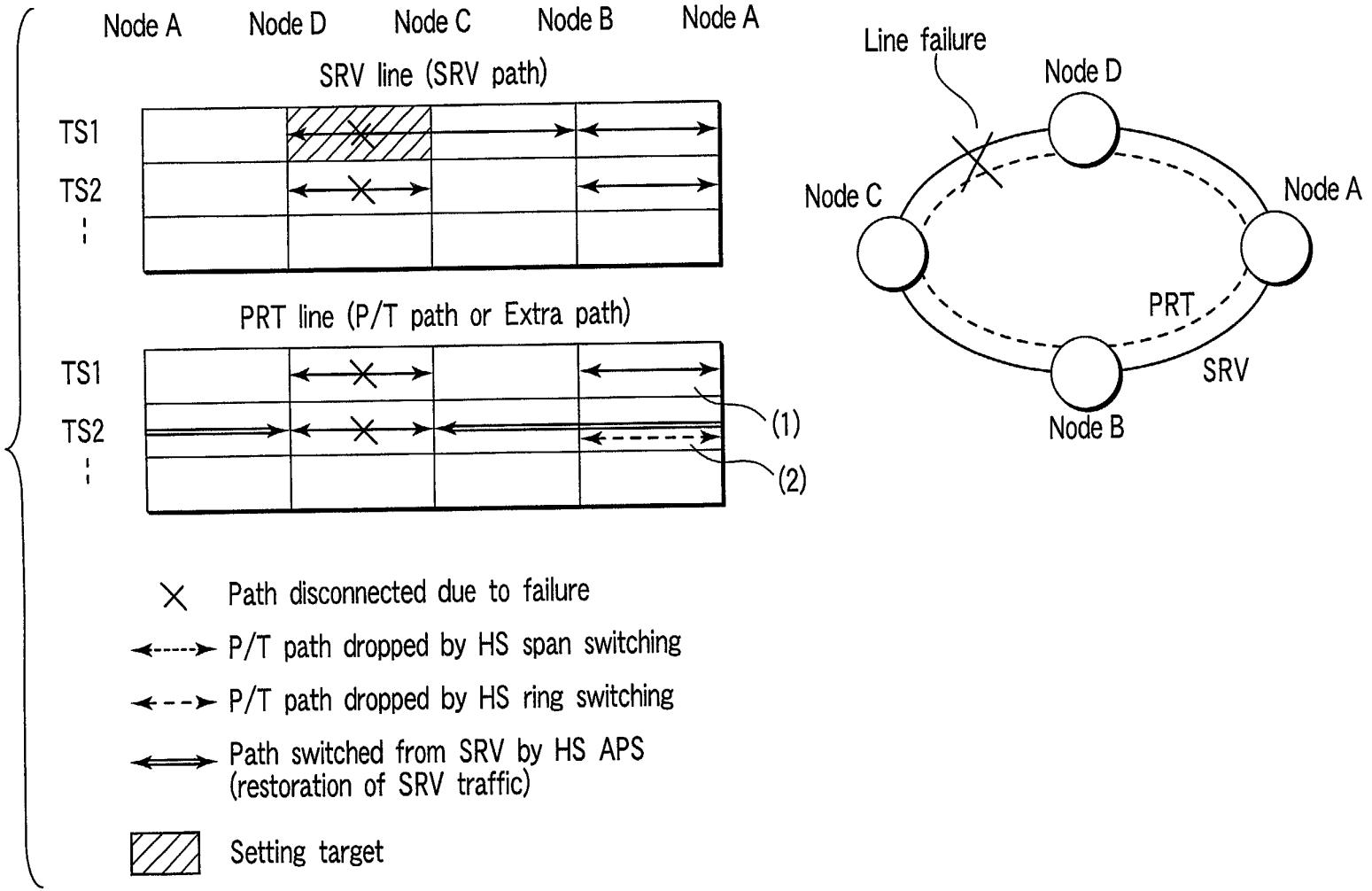

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 37

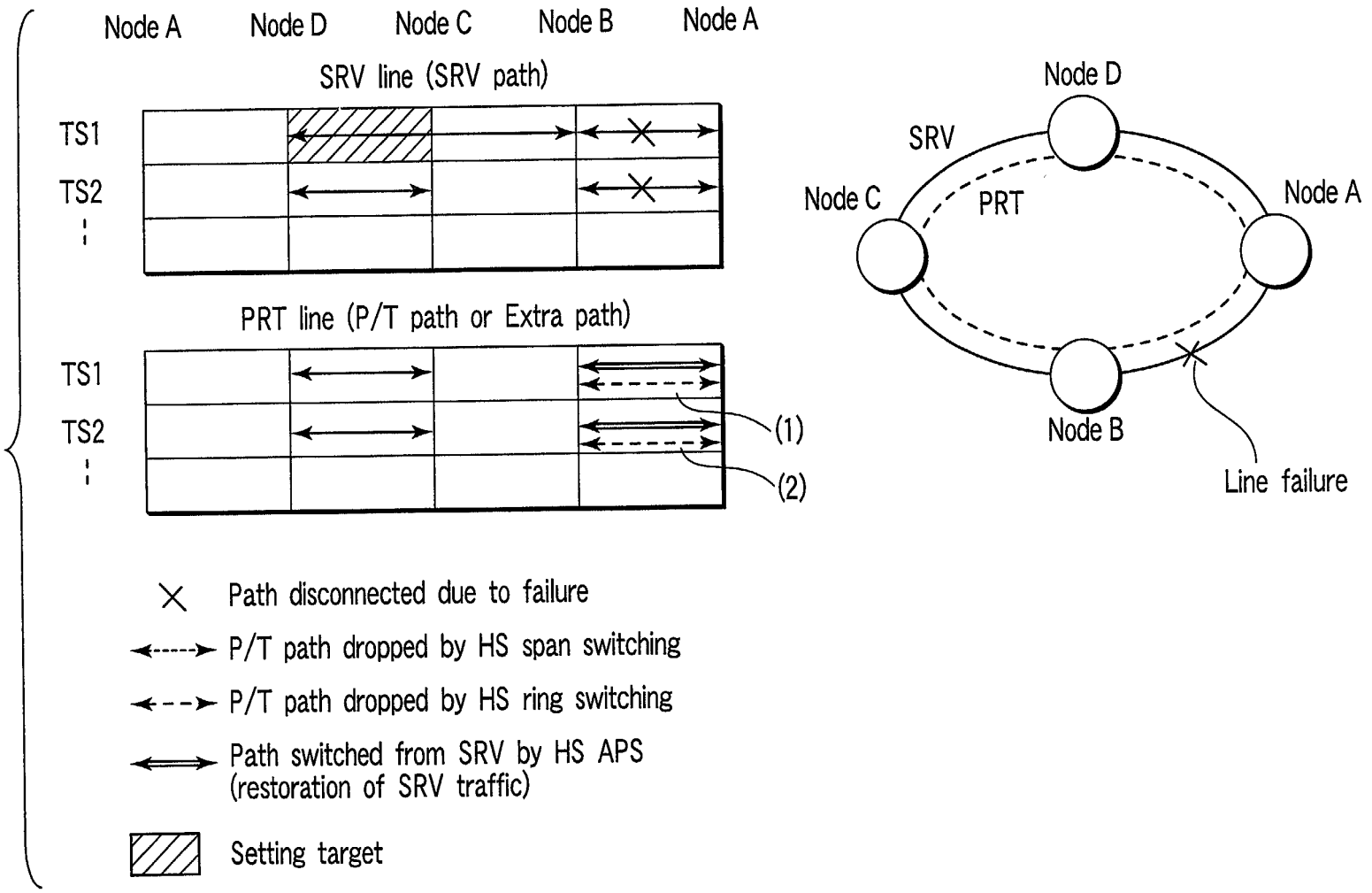

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Node D
SRV
Node C
PRT
Node A
Node B
Line failure

FIG. 38

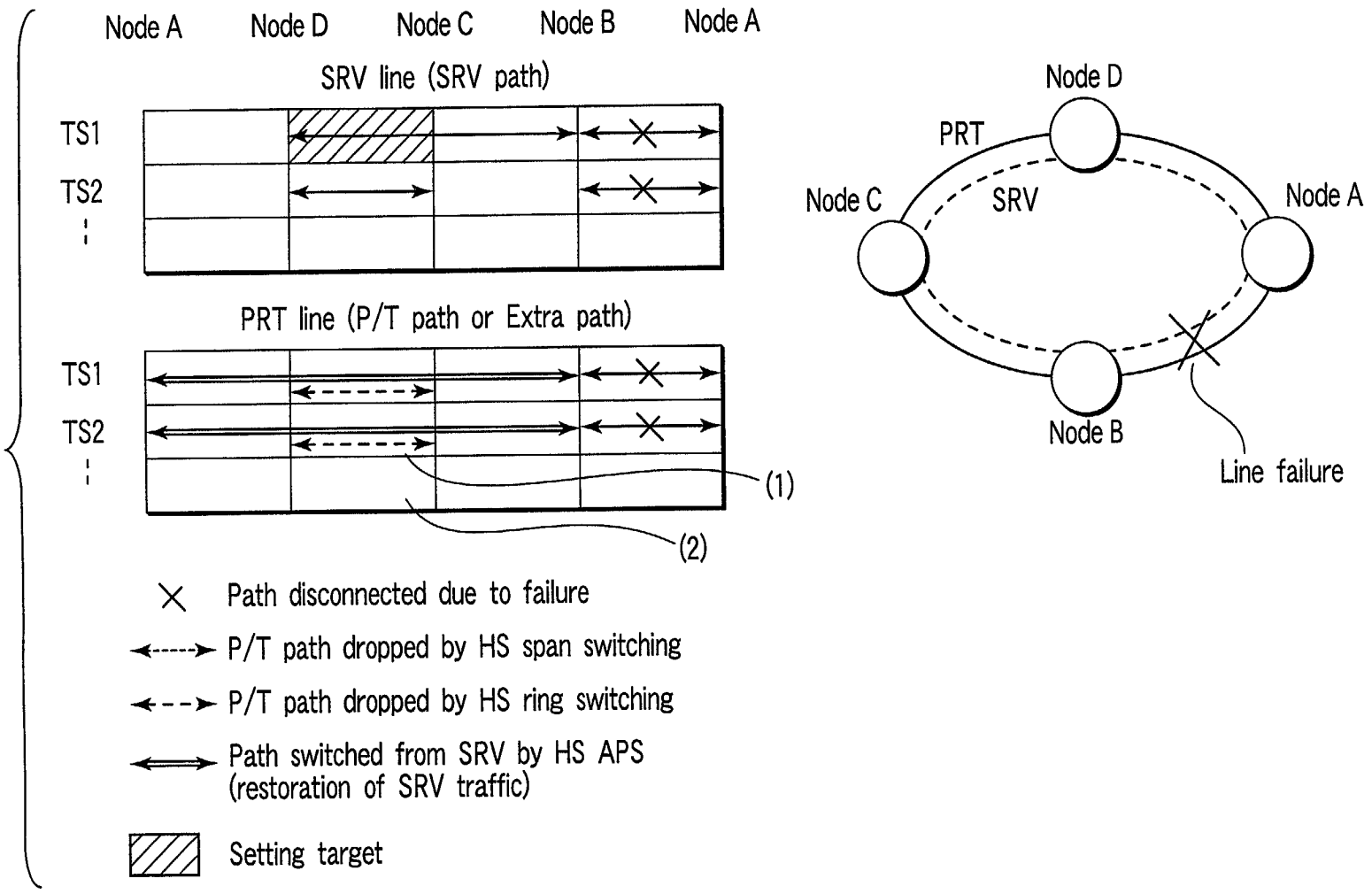

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Node D
PRT
Node C
SRV
Node A
Node B
Line failure

FIG. 39

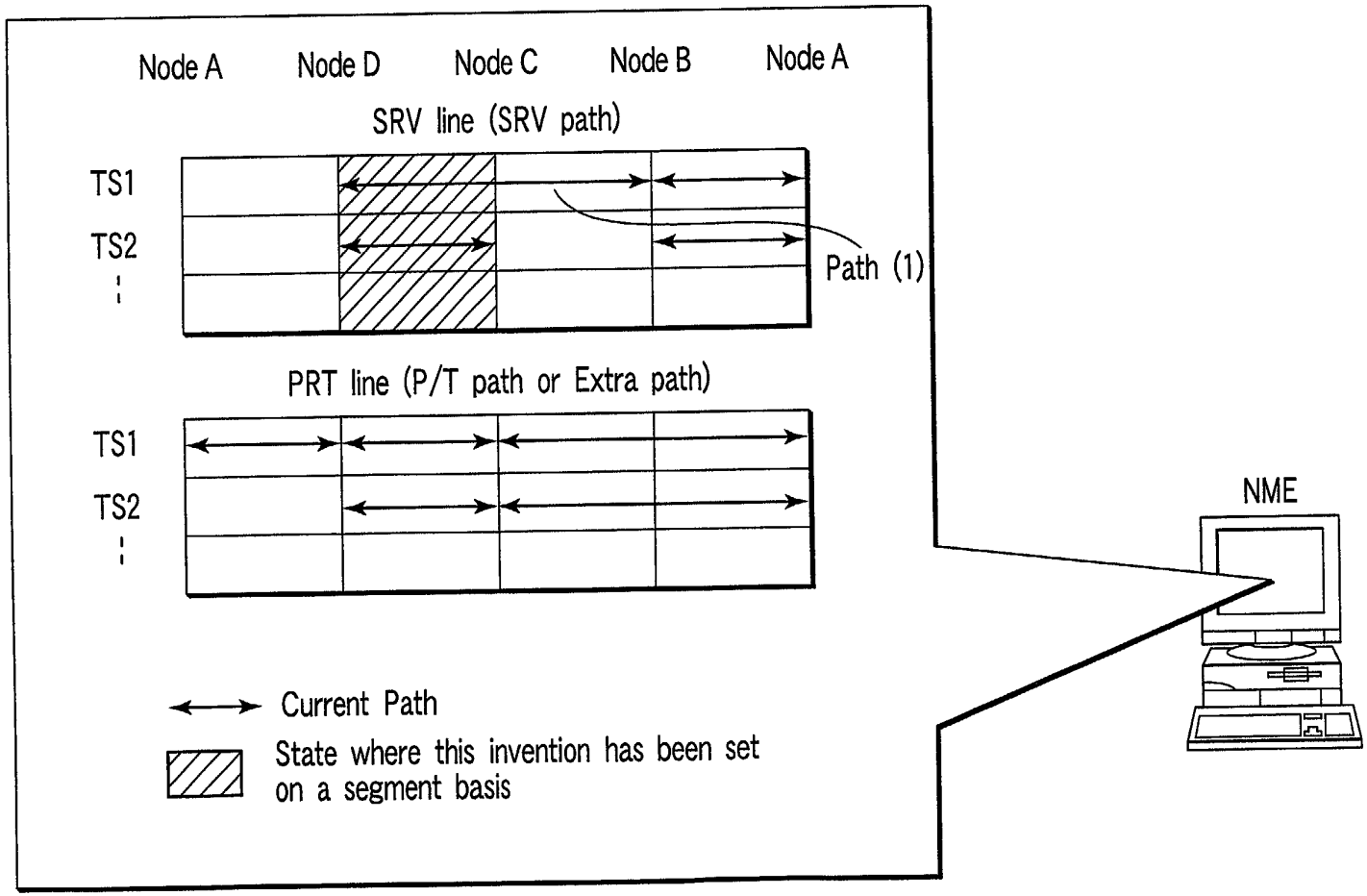

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
Path (1)
PRT line (P/T path or Extra path)
TS1
TS2
NME
Current Path
State where this invention has been set on a segment basis

FIG. 40

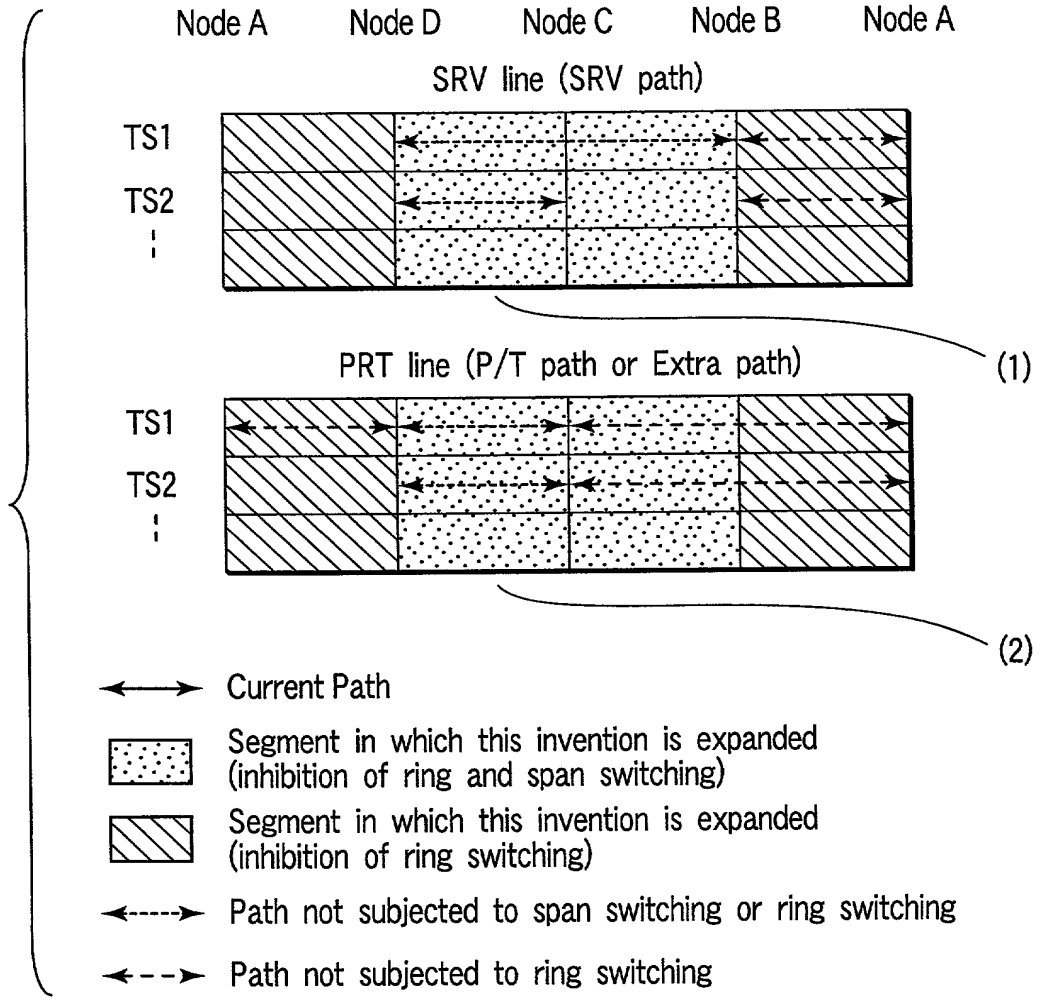
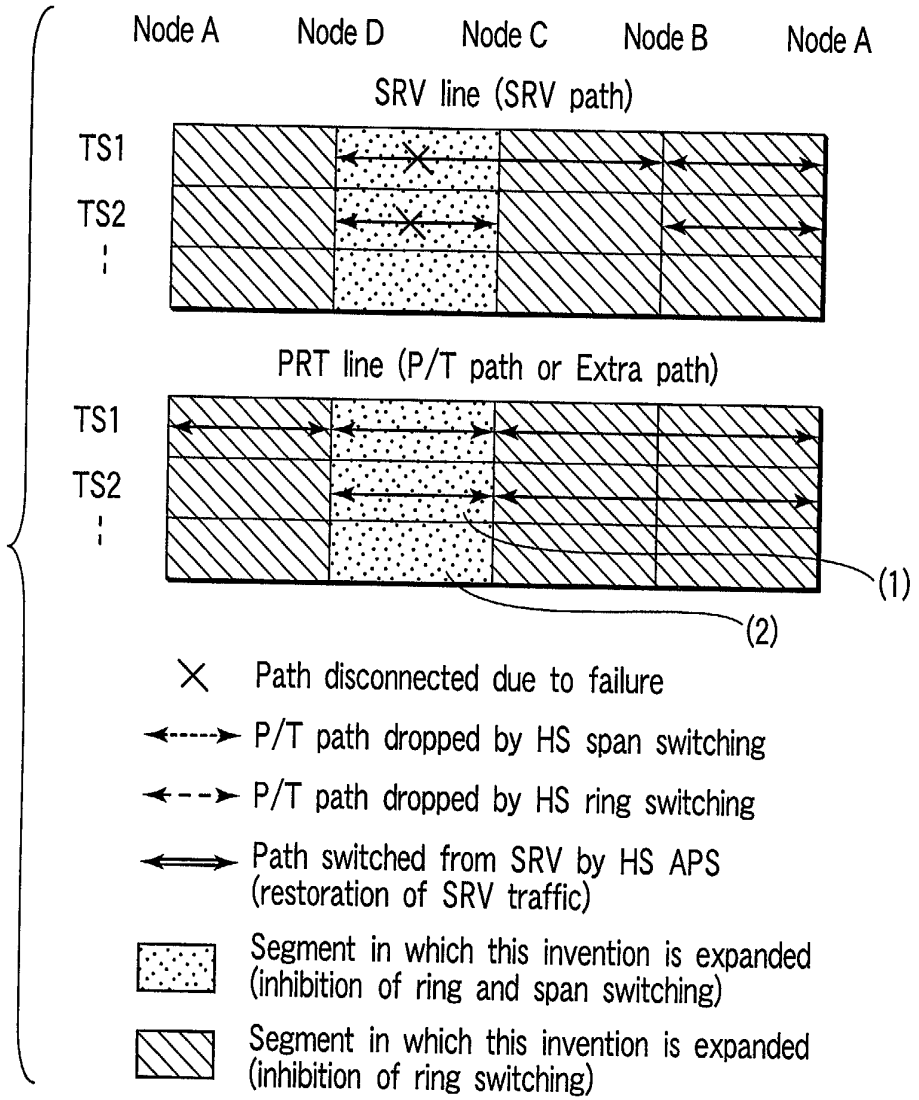

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
(1)
PRT line (P/T path or Extra path)
TS1
TS2
(2)
Current Path
Segment in which this invention is expanded (inhibition of ring and span switching)
Segment in which this invention is expanded (inhibition of ring switching)
Path not subjected to span switching or ring switching
Path not subjected to ring switching

FIG. 41

	Node	D				C				B				A			
	West/East	W		E		W		E		W		E		W		E	
	Span/Ring	S	R	S	R	S	R	S	R	S	R	S	R	S	R	S	R
Timeslot	TS1	0	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1
	TS2	0	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1
	TS3	0	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1
	TS4	0	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1
	•							•									
	•							•									
	•							•									
	TS64	0	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1

FIG. 42


Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)

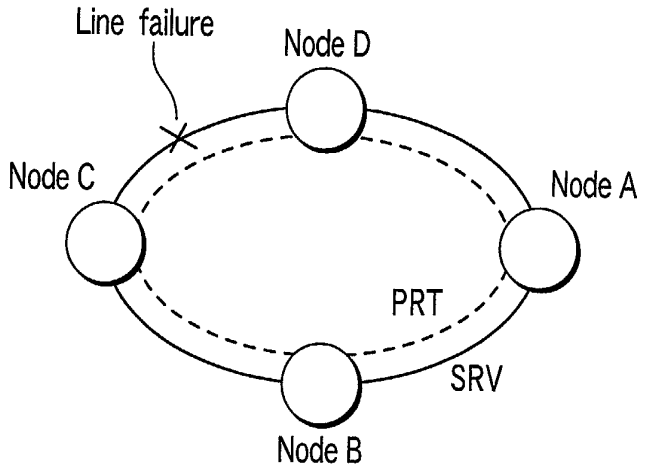

Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 43

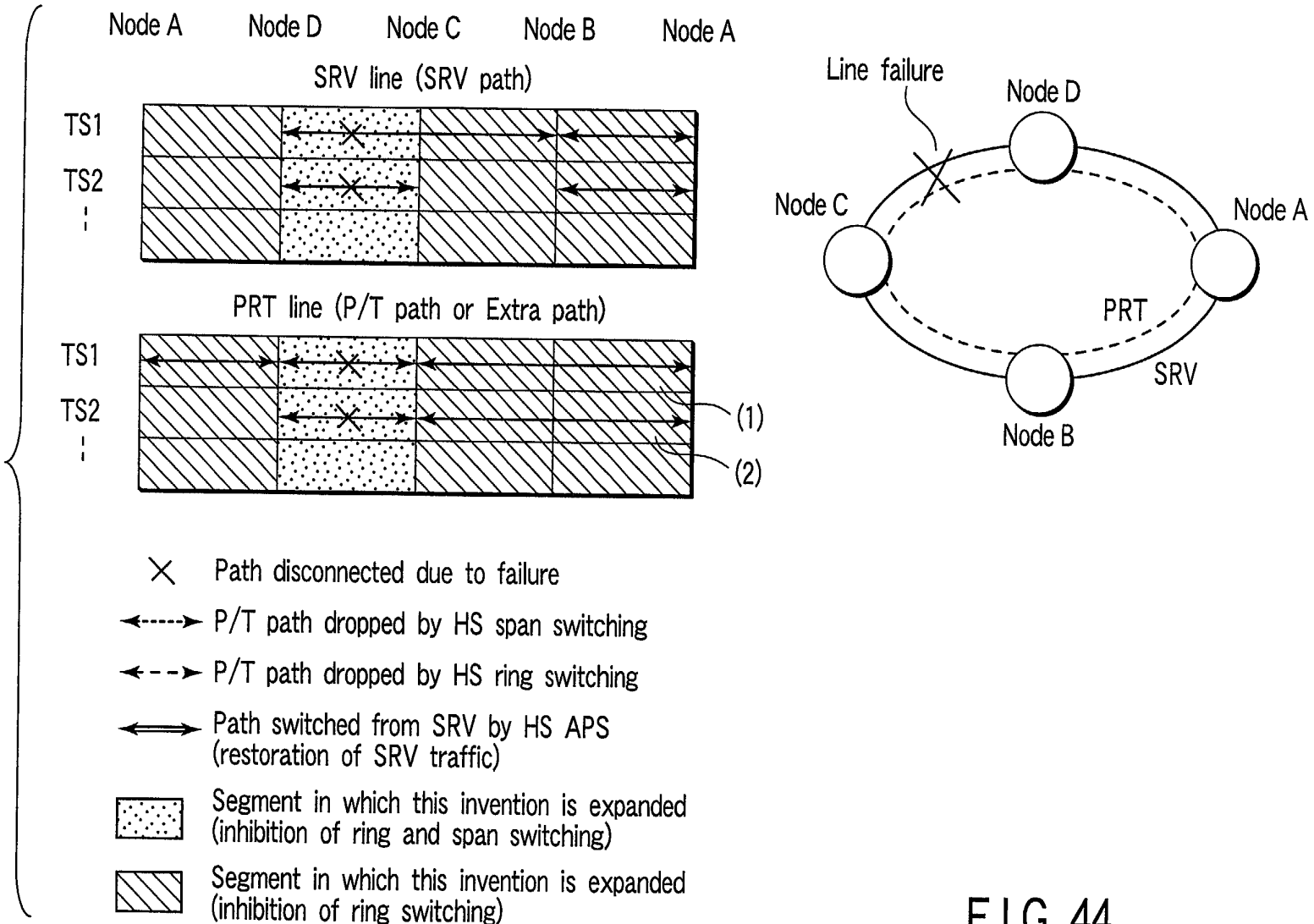
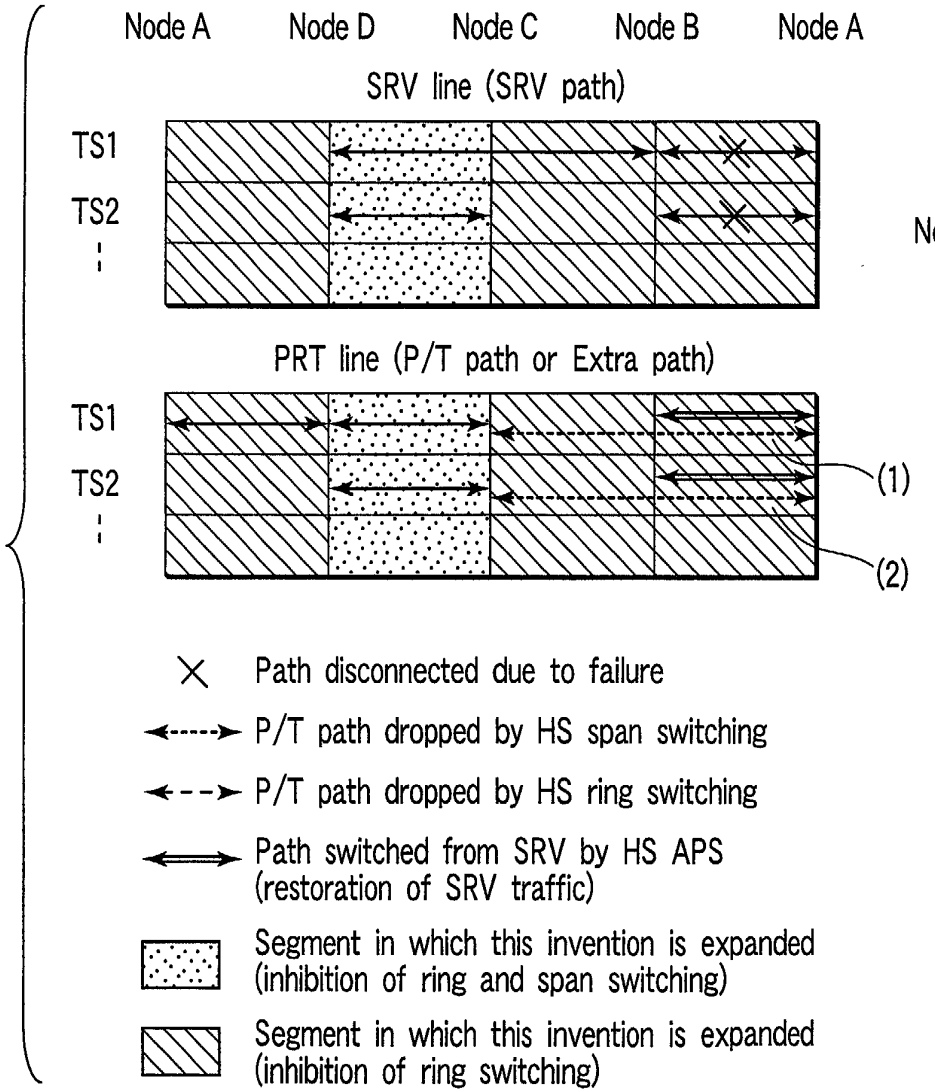

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 44


Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)

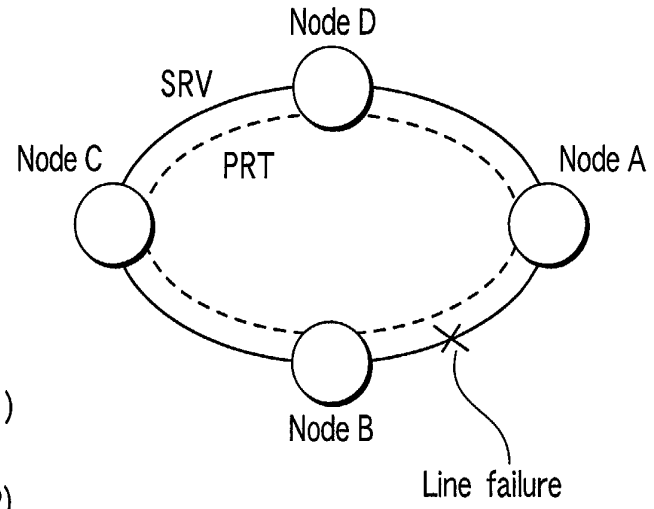
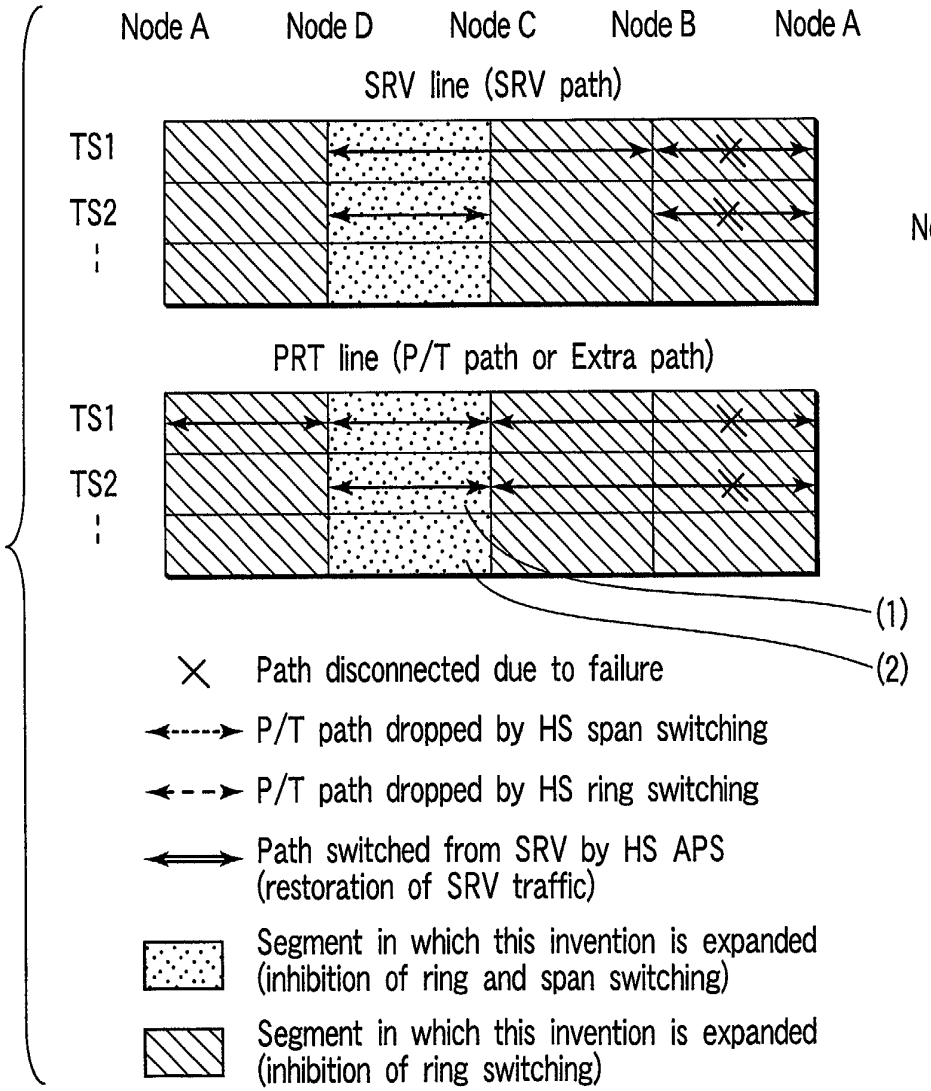

Node D
SRV
Node C
PRT
Node A
Node B
Line failure

FIG. 45


Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)

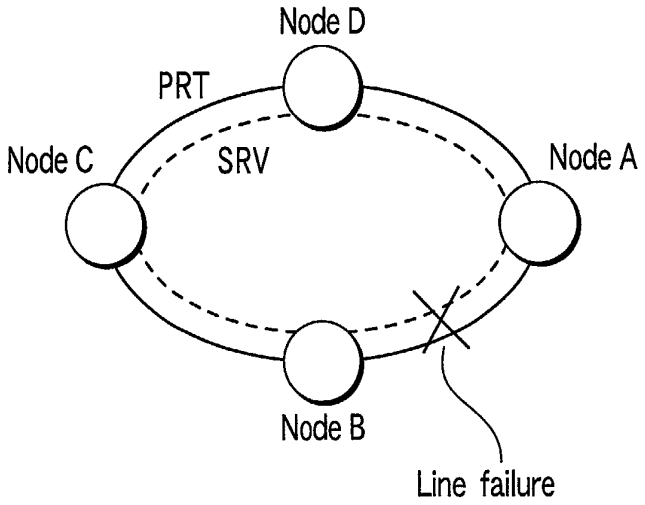

Node D
PRT
Node C
SRV
Node A
Node B
Line failure

FIG. 46

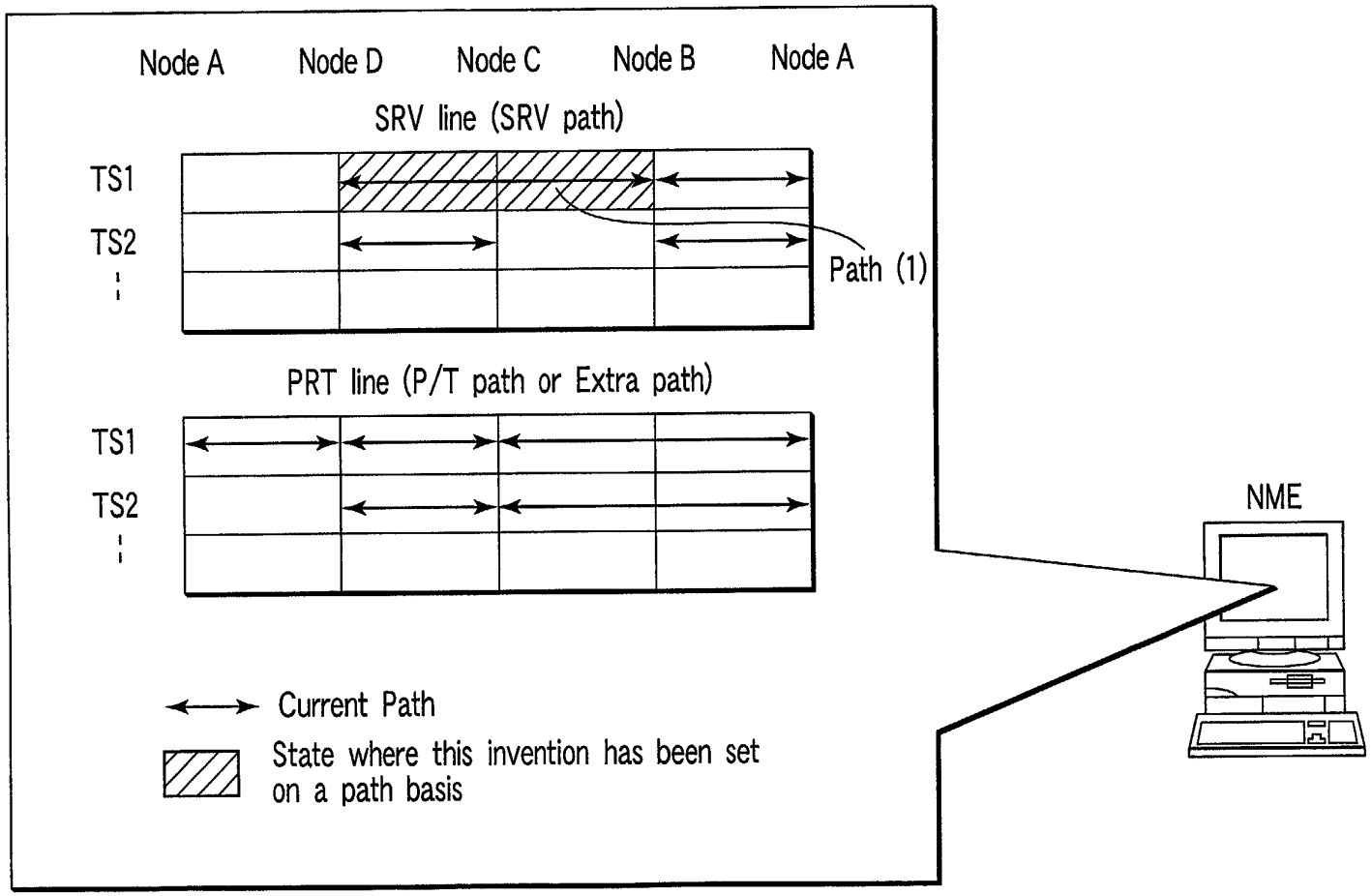

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
Path (1)
PRT line (P/T path or Extra path)
TS1
TS2
NME
Current Path
State where this invention has been set on a path basis

FIG. 47

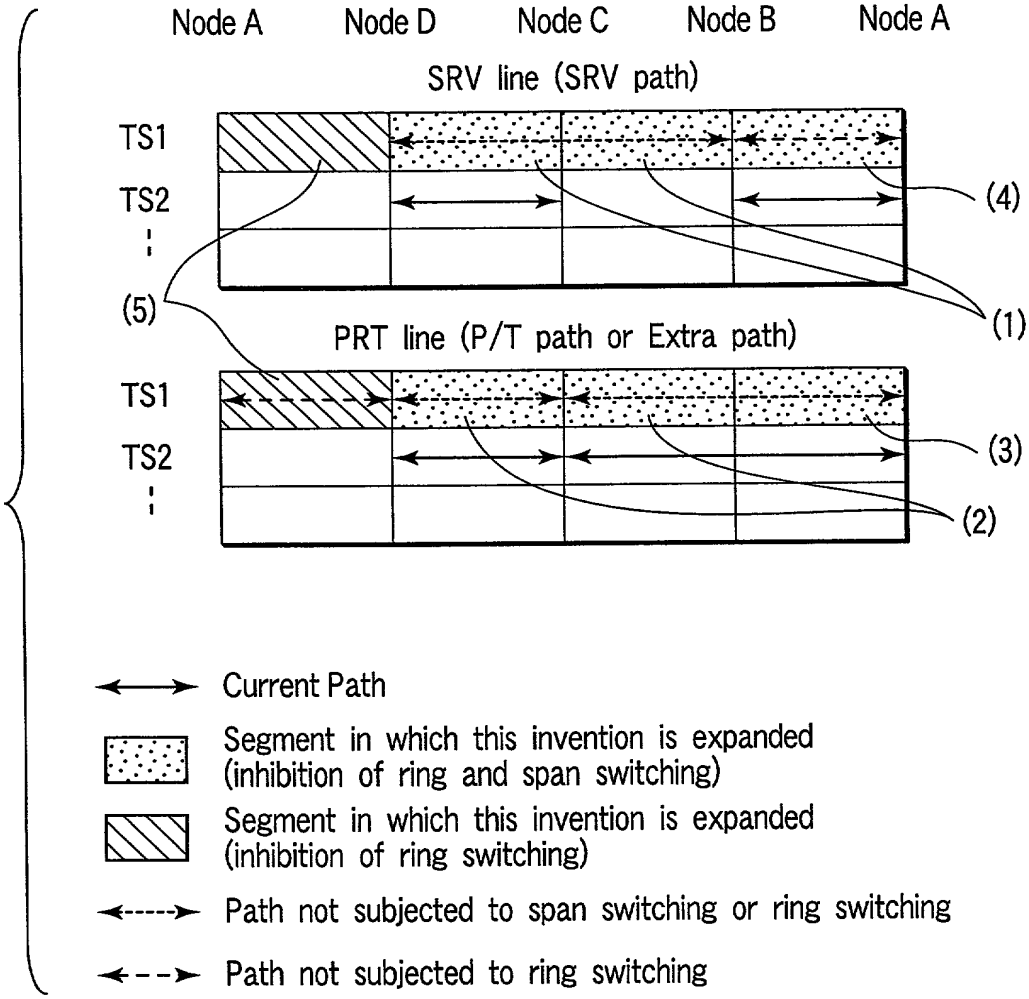


FIG. 48

	Node	D				C				B				A			
	West/East	W		E		W		E		W		E		W		E	
	Span/Ring	S	R	S	R	S	R	S	R	S	R	S	R	S	R	S	R
Timeslot	TS1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	TS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	•																
	•																
	•																
	TS64	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIG. 49

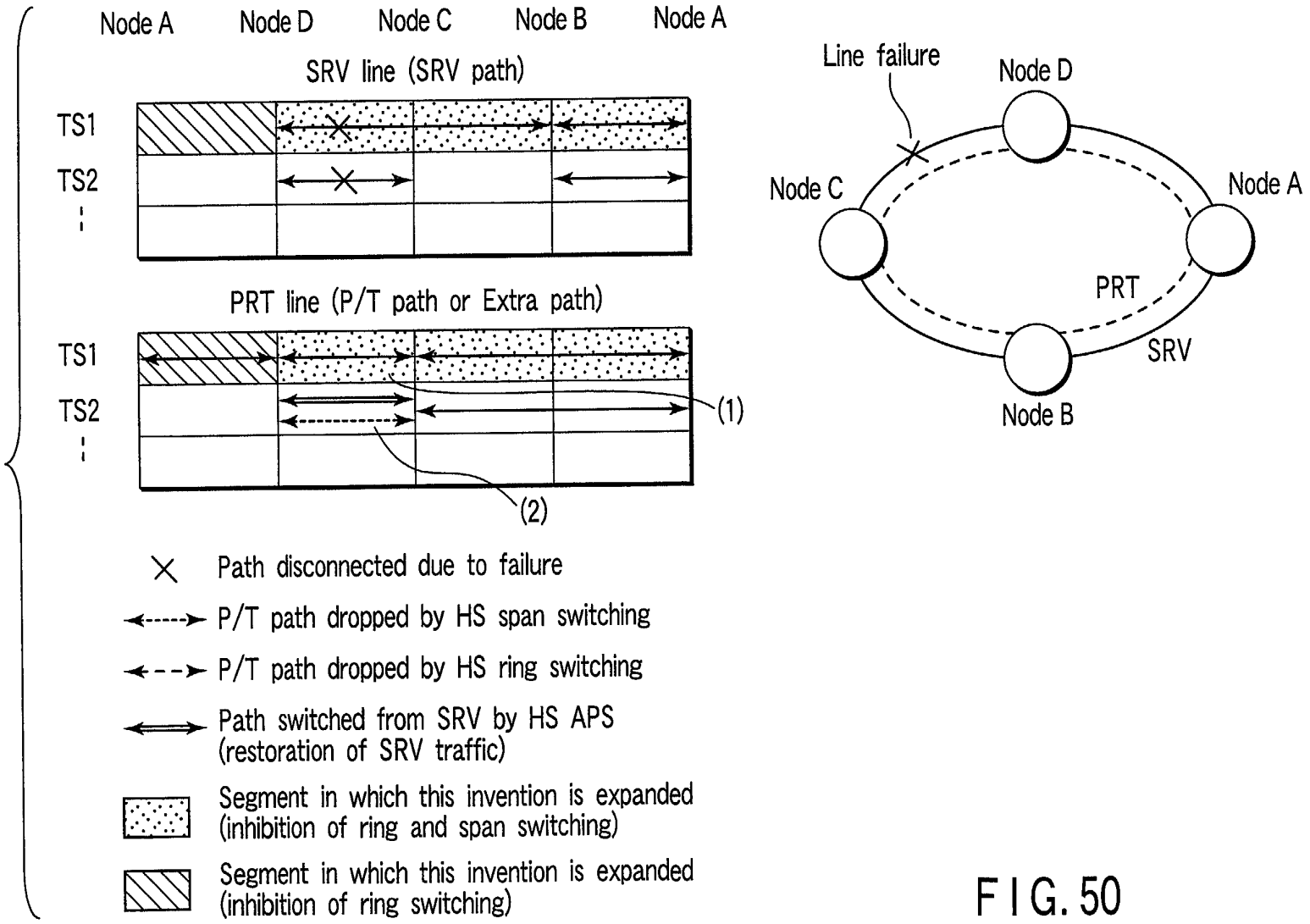

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 50

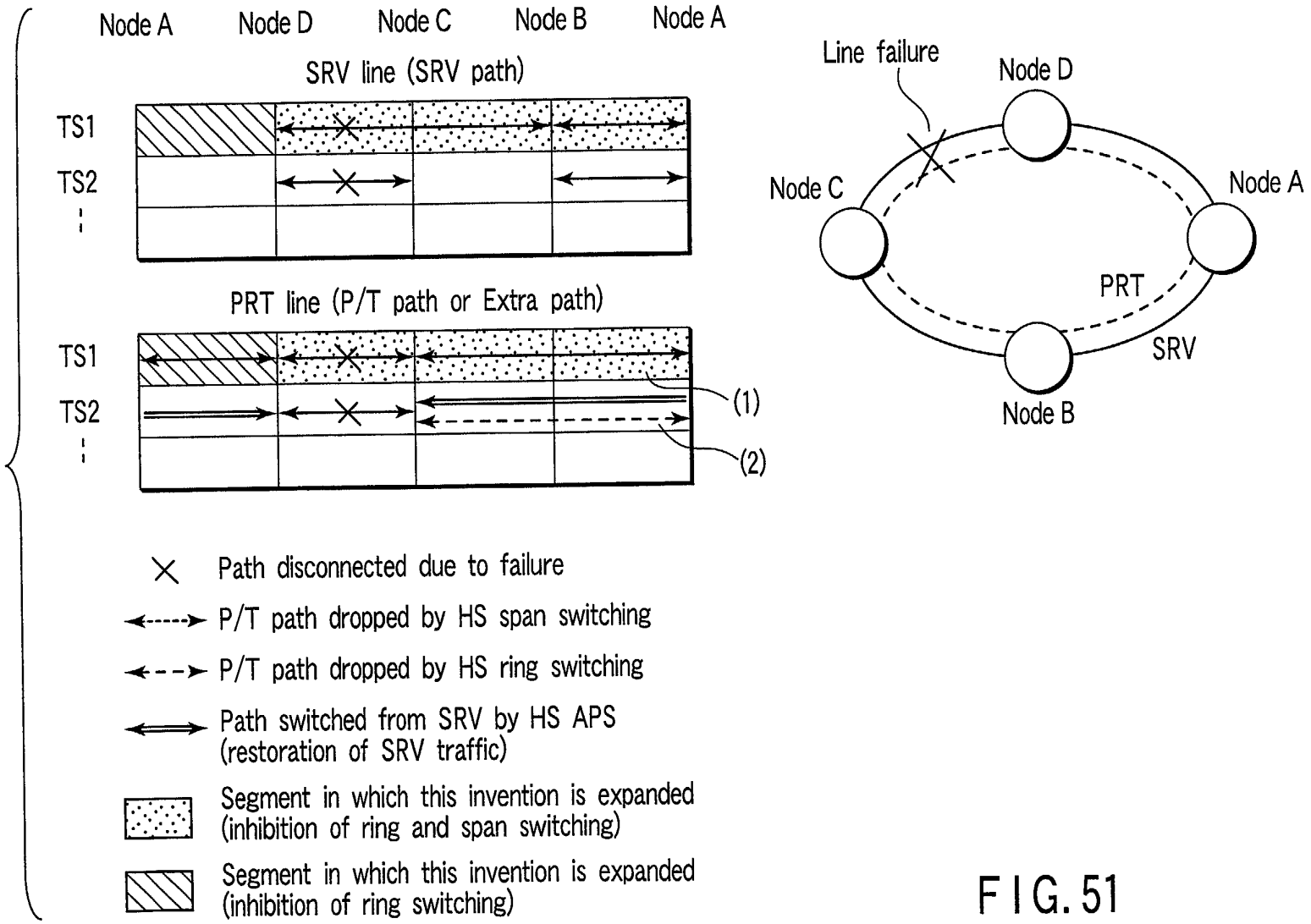

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 51

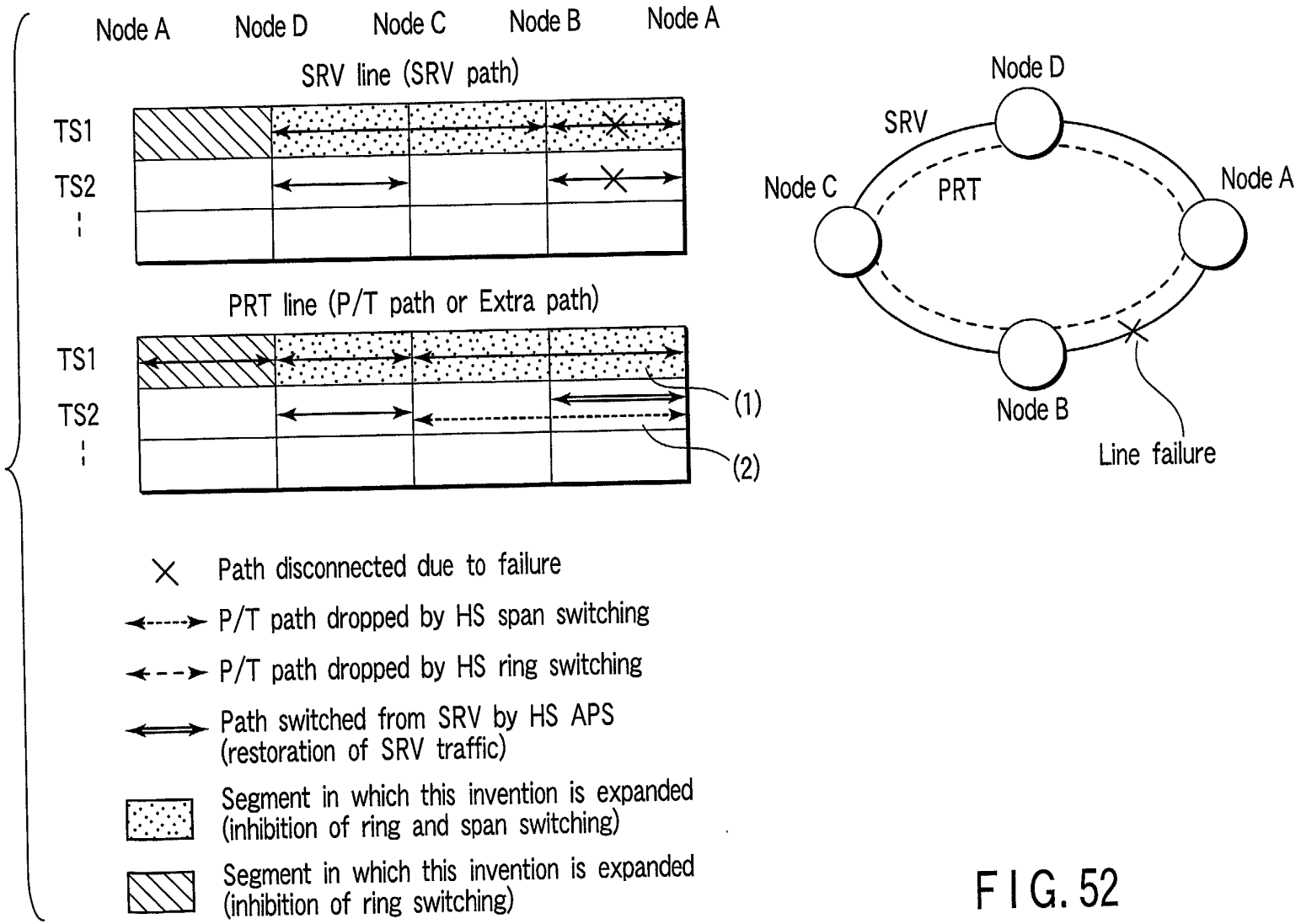
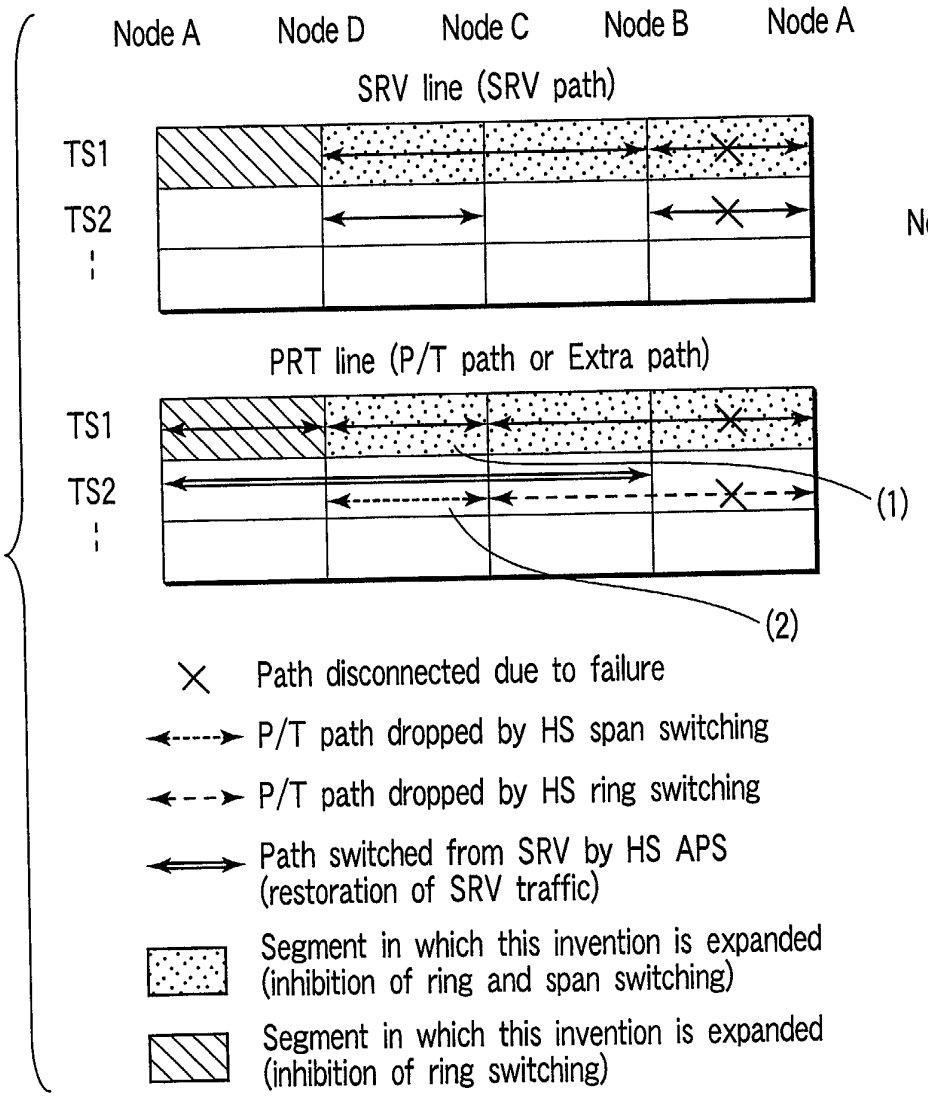

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)
Node D
SRV
Node C
PRT
Node A
Node B
Line failure

FIG. 52


Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)

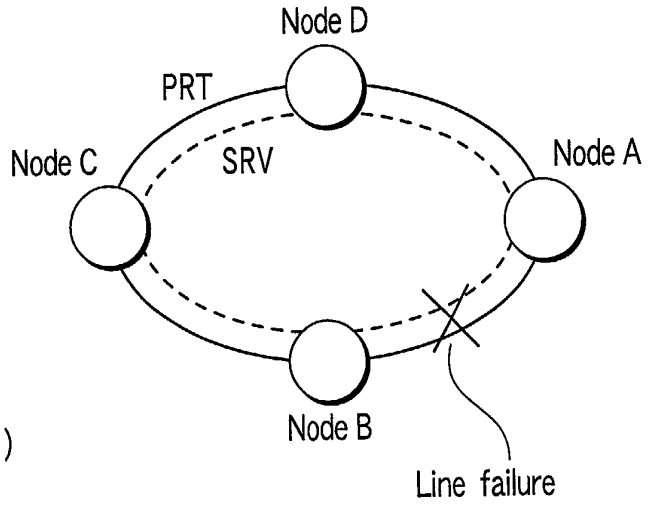

Node D
PRT
Node C
SRV
Node A
Node B
Line failure

FIG. 53

	Node	D				C				B				A			
	West/East	W		E		W		E		W		E		W		E	
	Span/Ring	S	R	S	R	S	R	S	R	S	R	S	R	S	R	S	R
Timeslot	TS1	0	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	TS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	•								•								
	•								•								
	•								•								
	TS64	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIG. 54

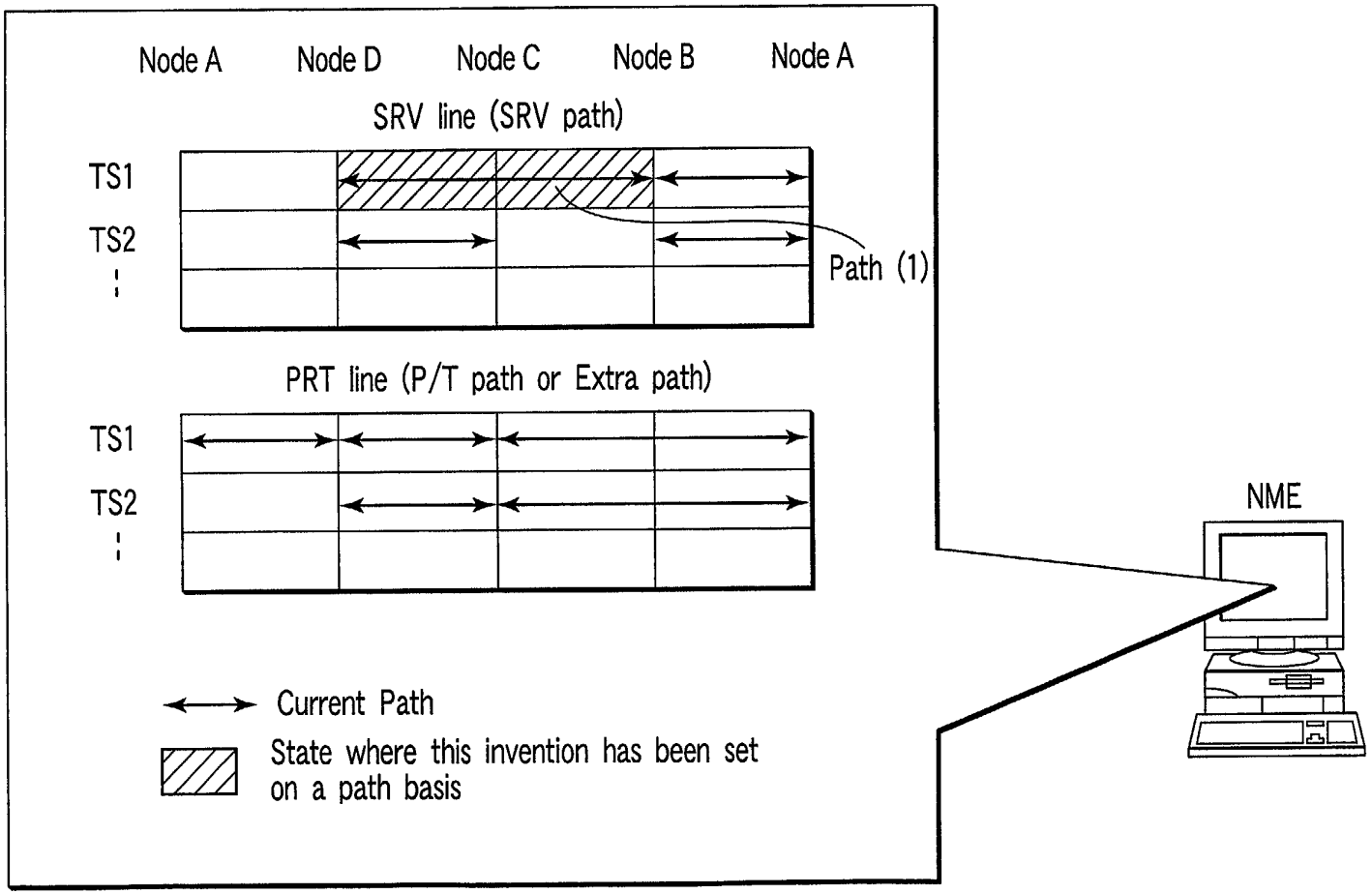

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
Path (1)
PRT line (P/T path or Extra path)
TS1
TS2
NME
Current Path
State where this invention has been set on a path basis

FIG. 55

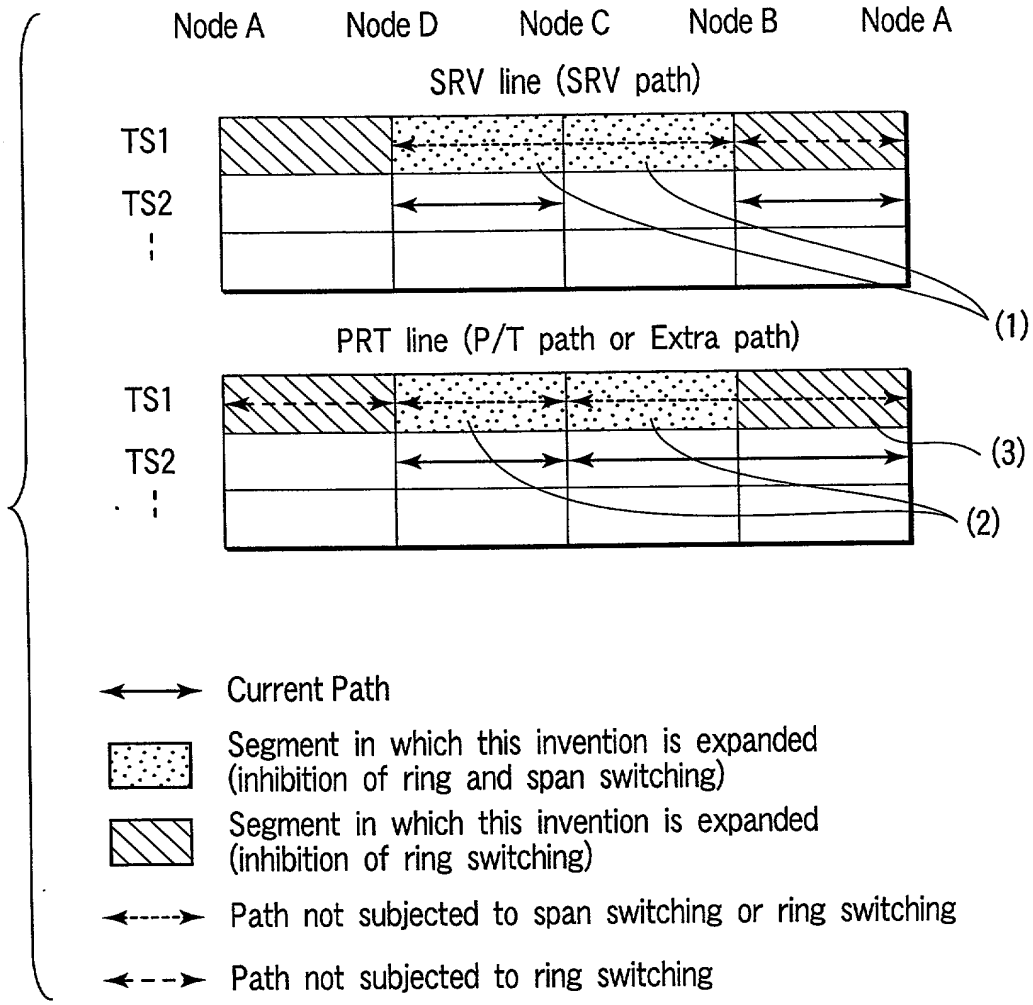
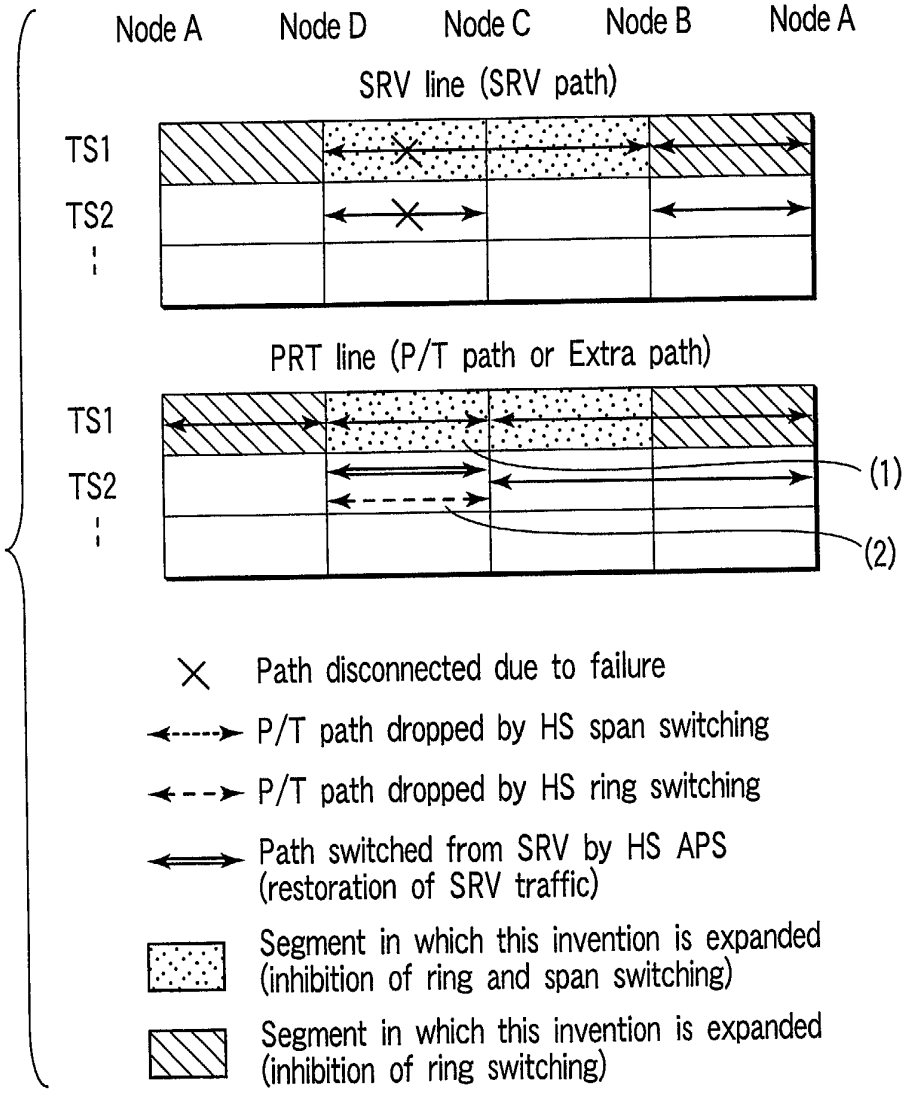

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
(1)
PRT line (P/T path or Extra path)
TS1
TS2
(3)
(2)
Current Path
Segment in which this invention is expanded (inhibition of ring and span switching)
Segment in which this invention is expanded (inhibition of ring switching)
Path not subjected to span switching or ring switching
Path not subjected to ring switching

FIG. 56


Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)

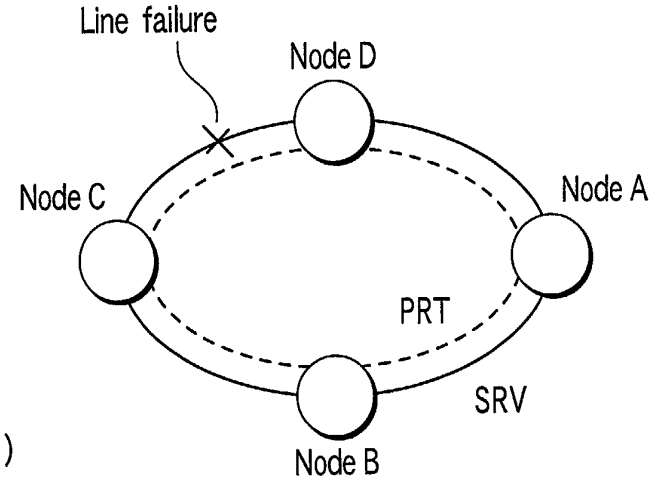

Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 57

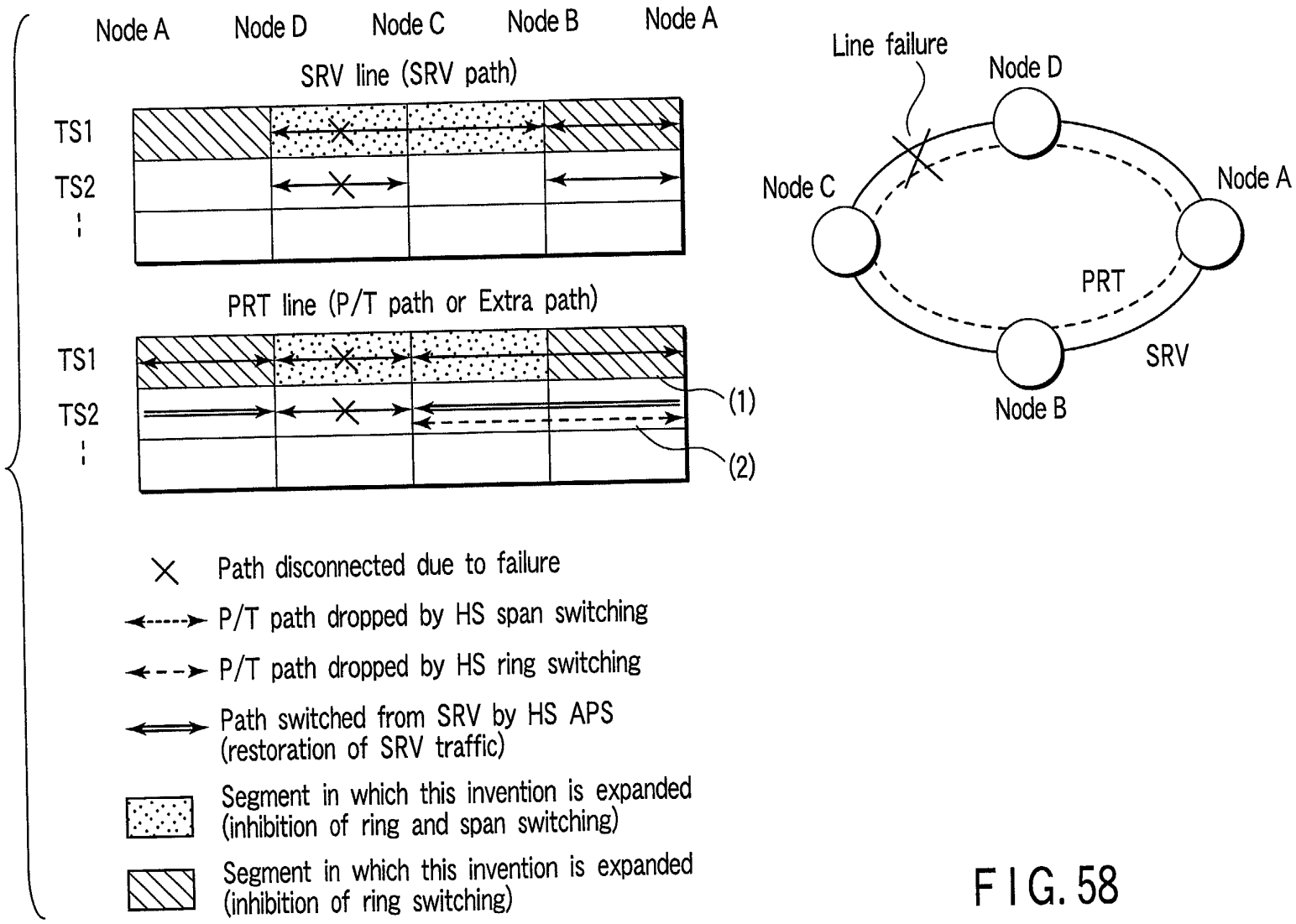

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 58

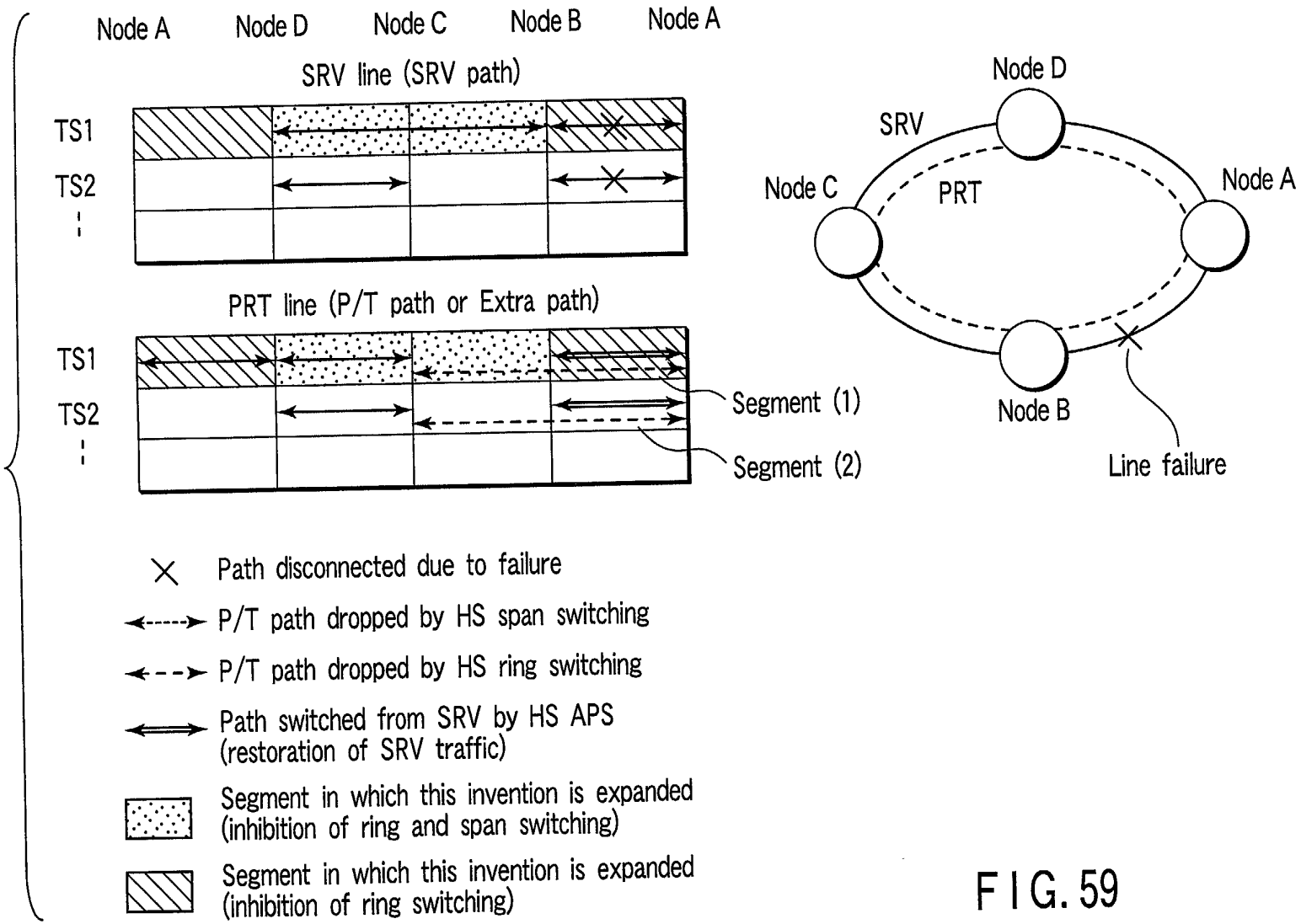

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Node D
SRV
Node C
PRT
Node A
Node B
Line failure
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)

FIG. 59

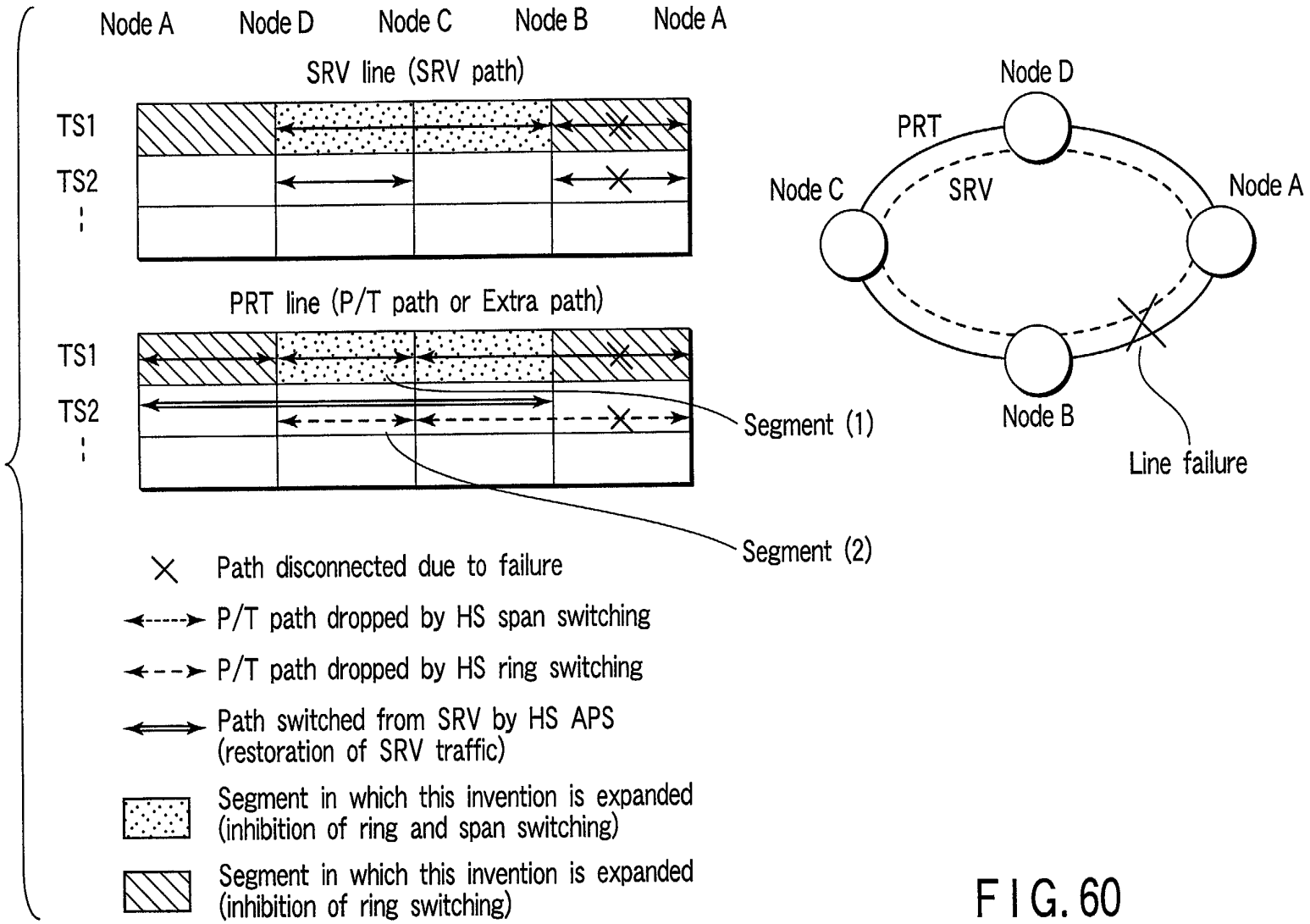

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)
Node D
PRT
Node C
SRV
Node A
Node B
Line failure

FIG. 60

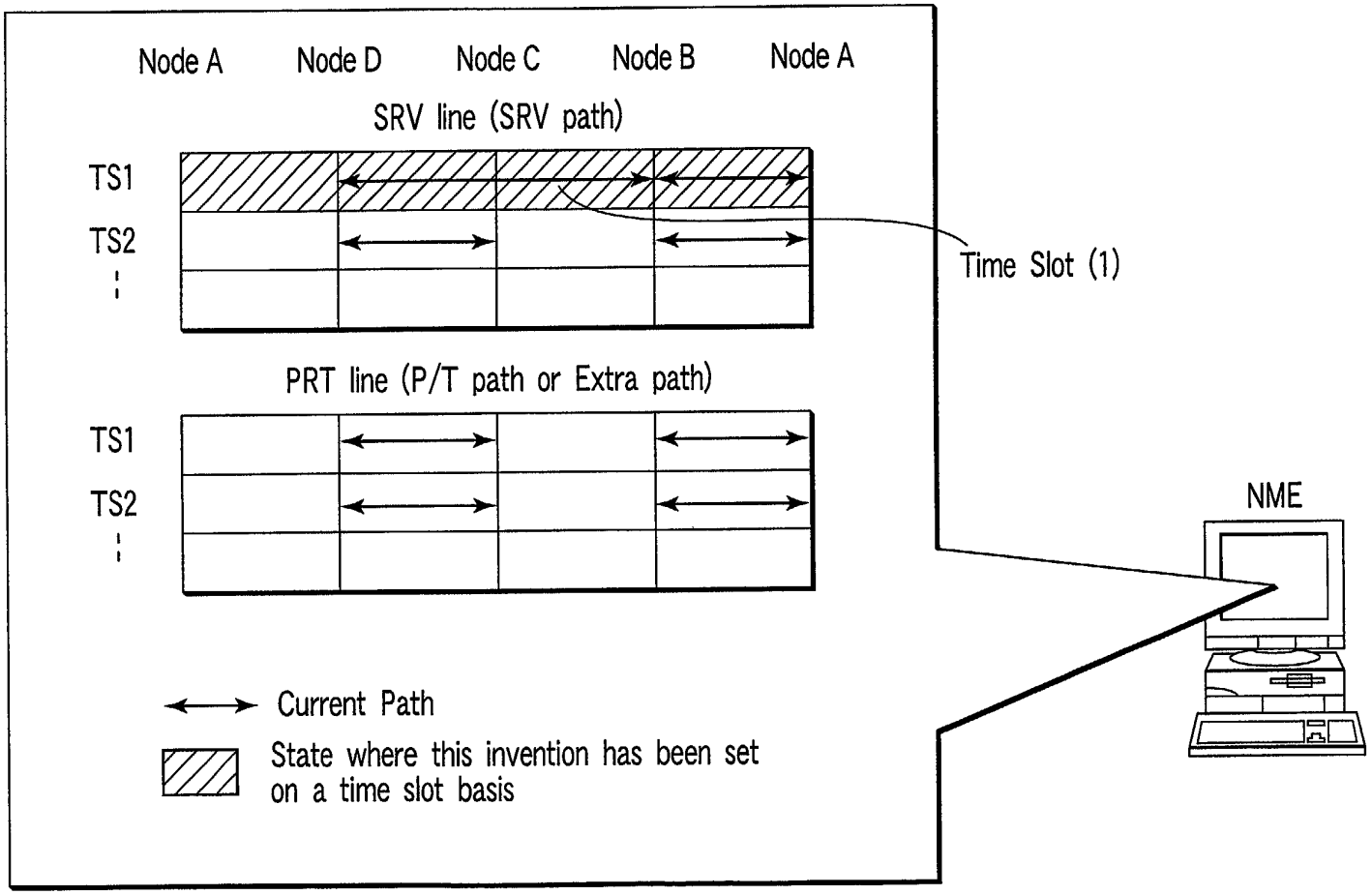

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
Time Slot (1)
PRT line (P/T path or Extra path)
TS1
TS2
NME
Current Path
State where this invention has been set on a time slot basis

FIG. 61

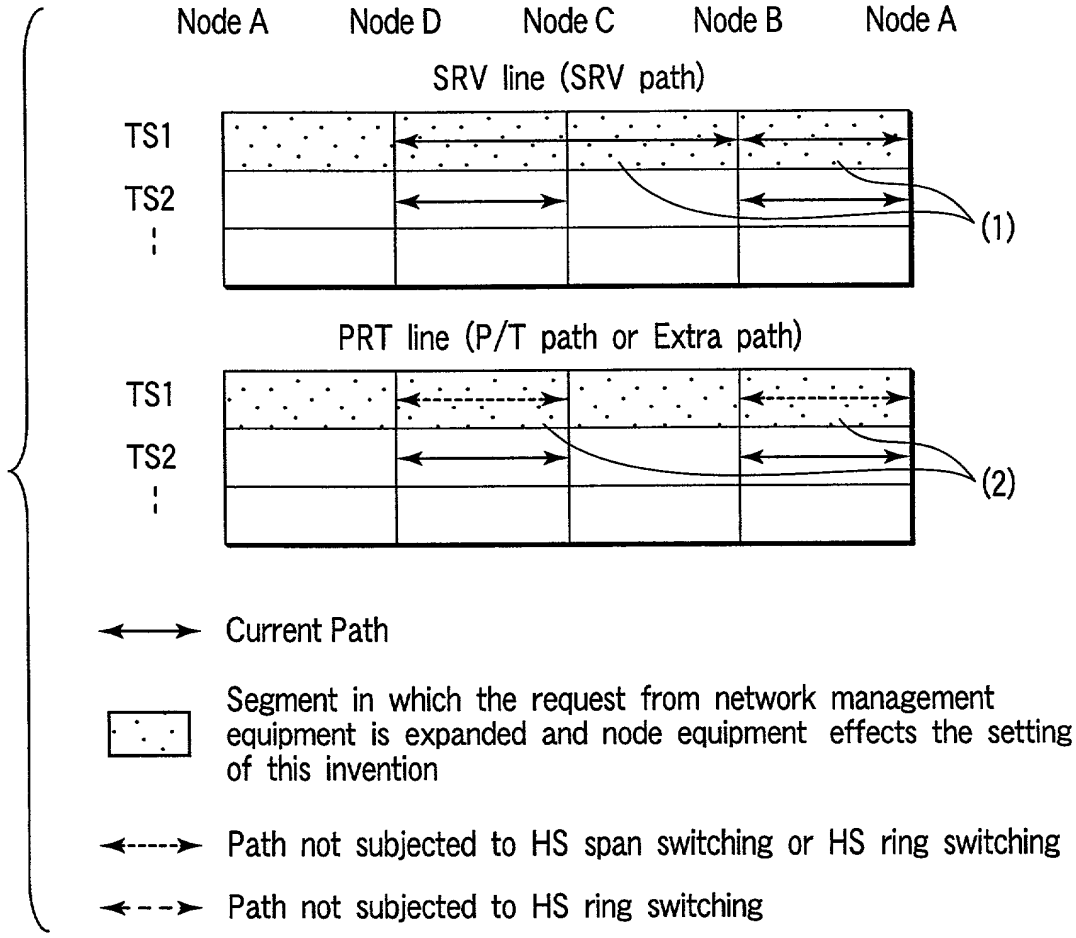


FIG. 62

	Node	D				C				B				A			
	West/East	W		E		W		E		W		E		W		E	
	Span/Ring	S	R	S	R	S	R	S	R	S	R	S	R	S	R	S	R
Timeslot	TS1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	TS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	•								•								
	•								•								
	•								•								
	TS64	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIG. 63

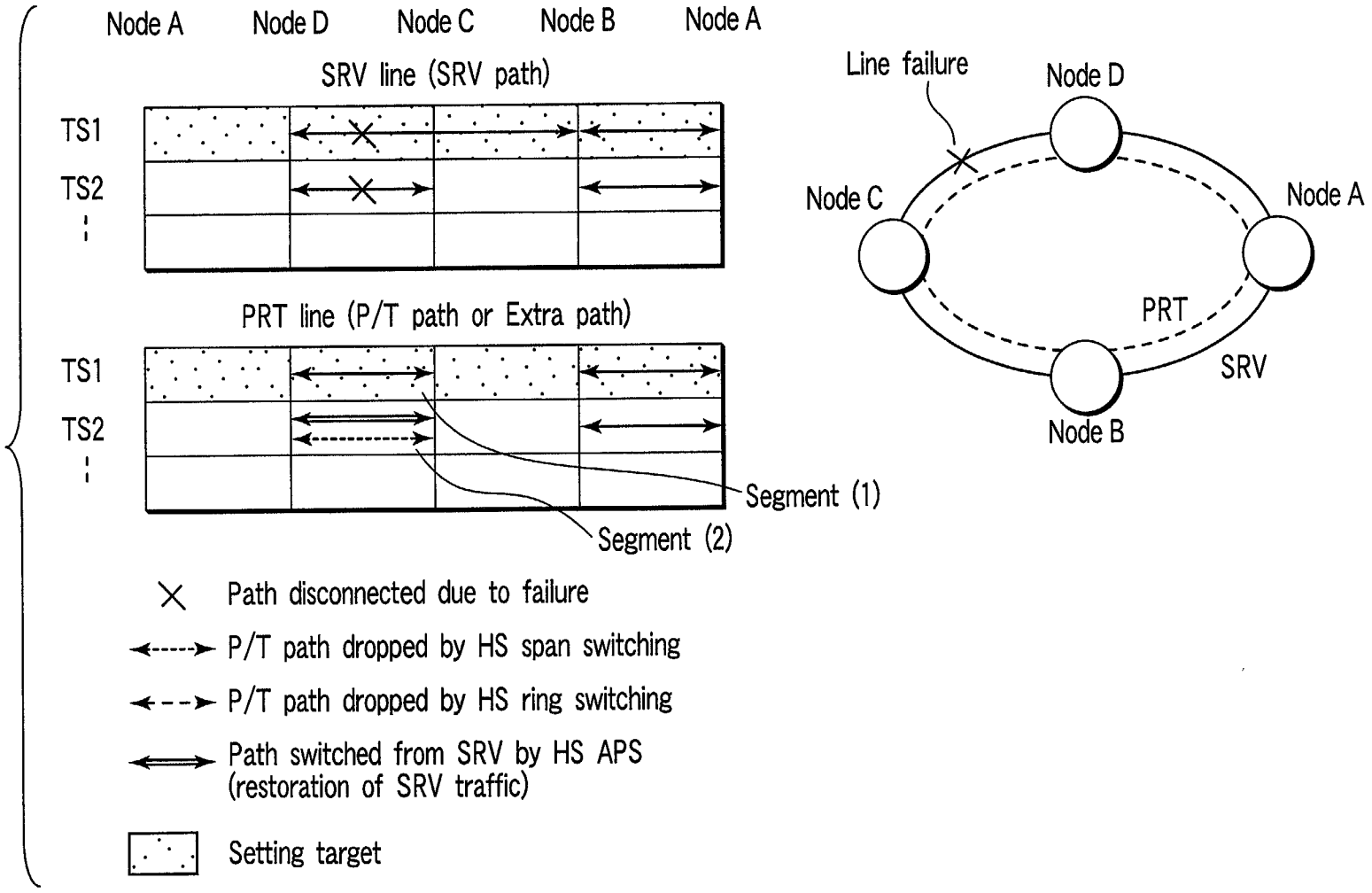

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 64

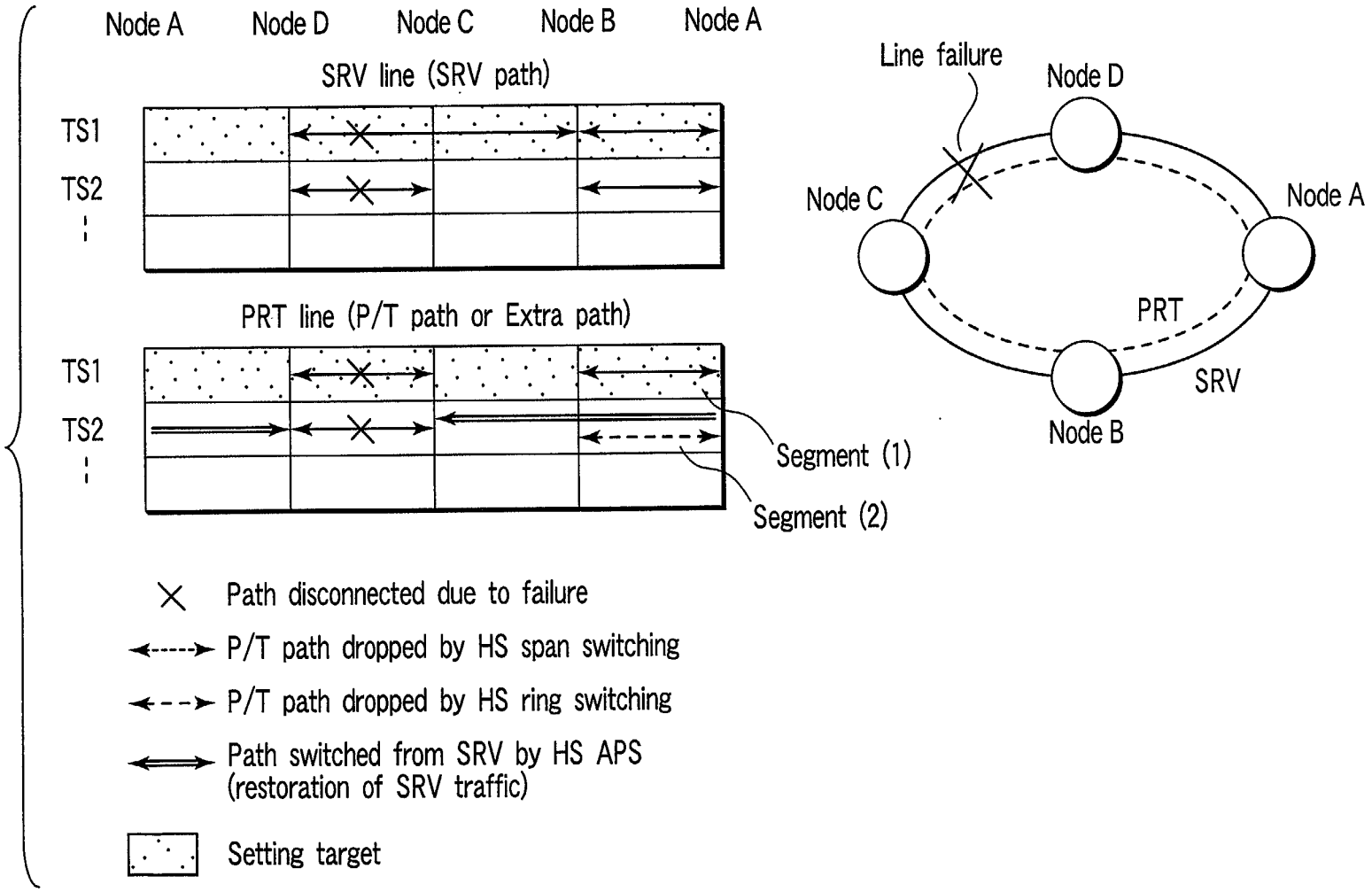

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 65

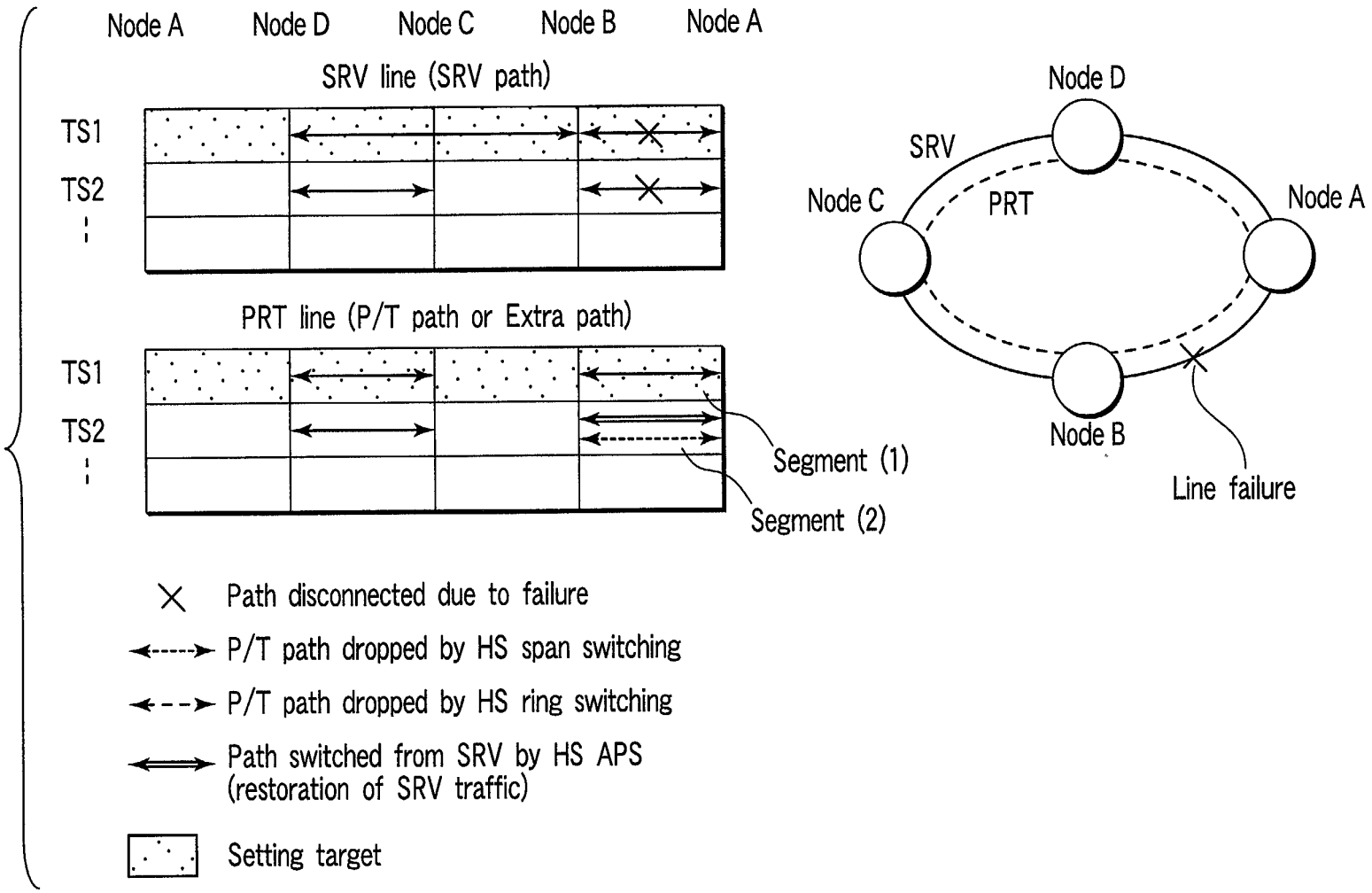

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Node D
SRV
Node C
PRT
Node A
Node B
Line failure
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target

FIG. 66

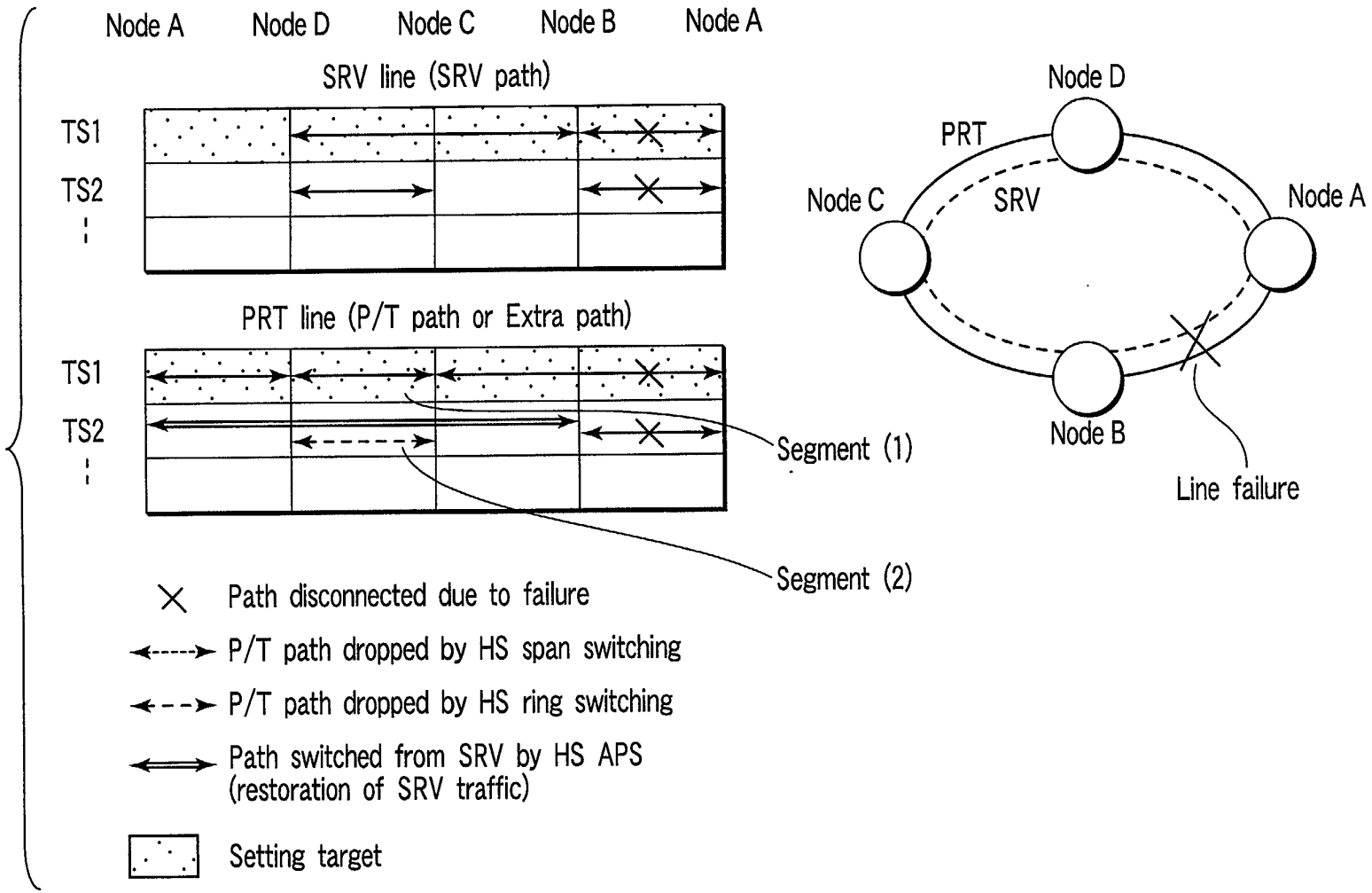

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Setting target
Node D
PRT
Node C
SRV
Node A
Node B
Line failure

FIG. 67

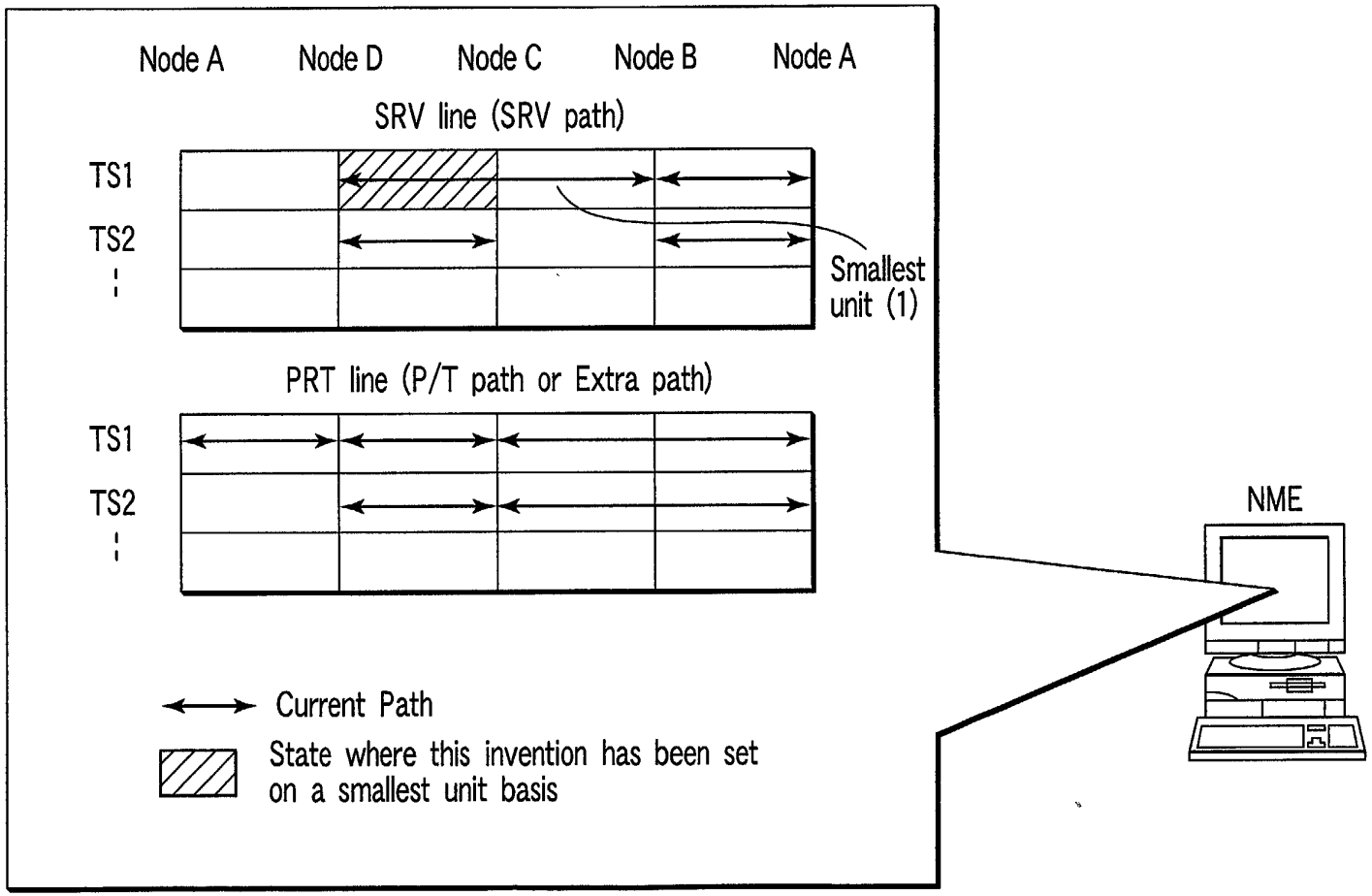

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
Smallest unit (1)
PRT line (P/T path or Extra path)
TS1
TS2
NME
Current Path
State where this invention has been set on a smallest unit basis

FIG. 68

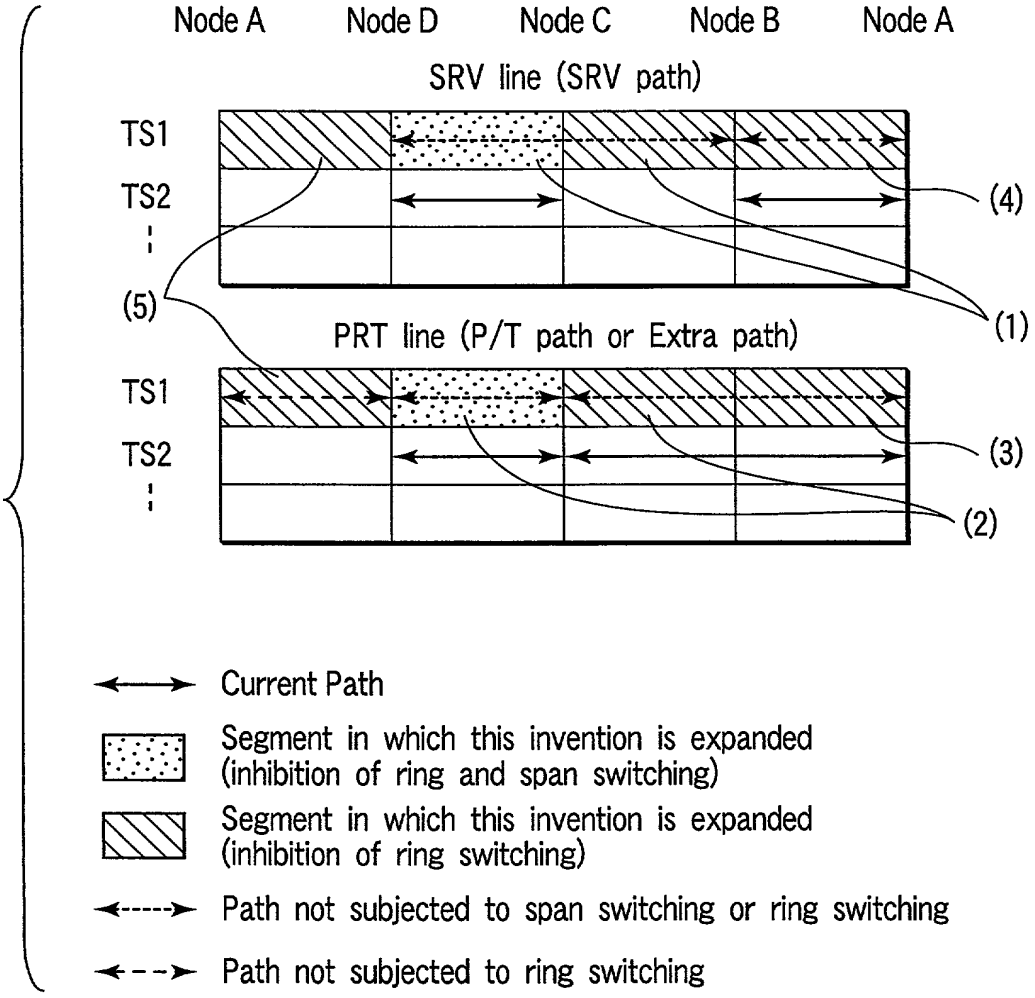
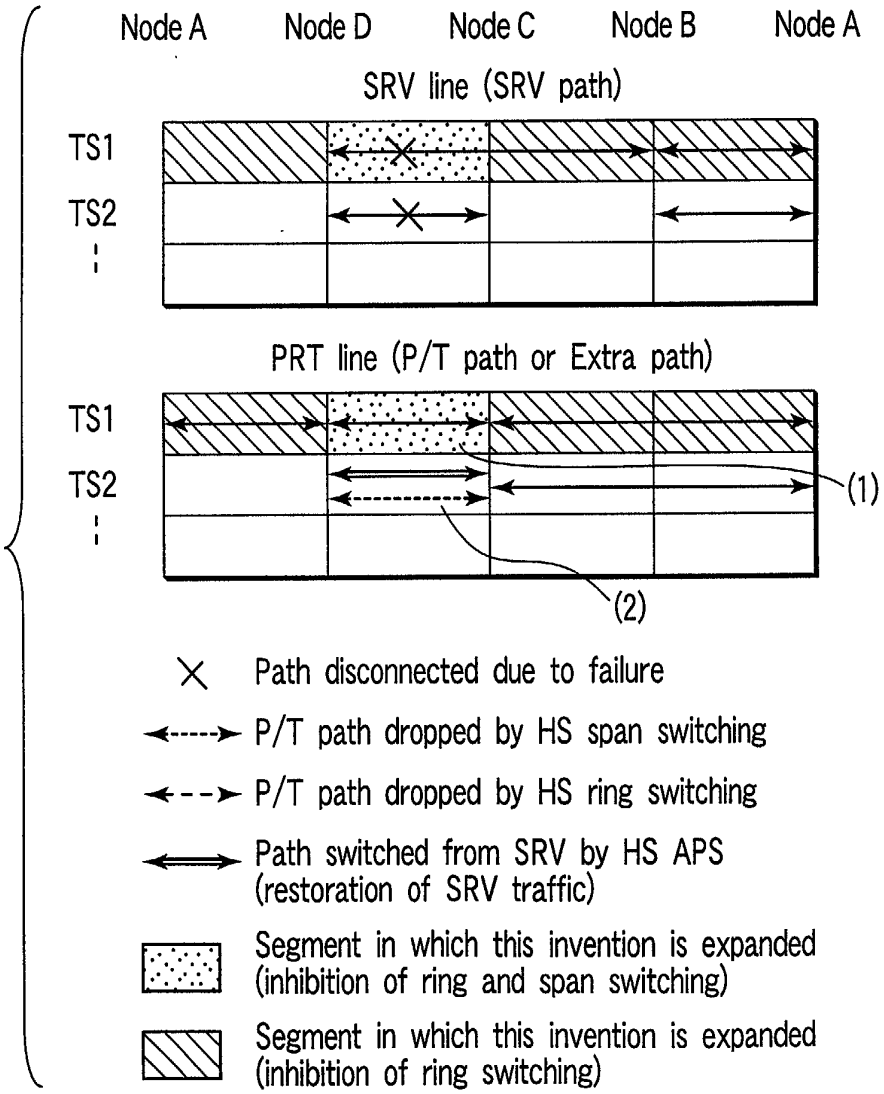


FIG. 69

	Node	D				C				B				A			
	West/East	W		E		W		E		W		E		W		E	
	Span/Ring	S	R	S	R	S	R	S	R	S	R	S	R	S	R	S	R
Timeslot	TS1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	TS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TS4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	•	•															
	•	•															
	•	•															
	TS64	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIG. 70


Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)

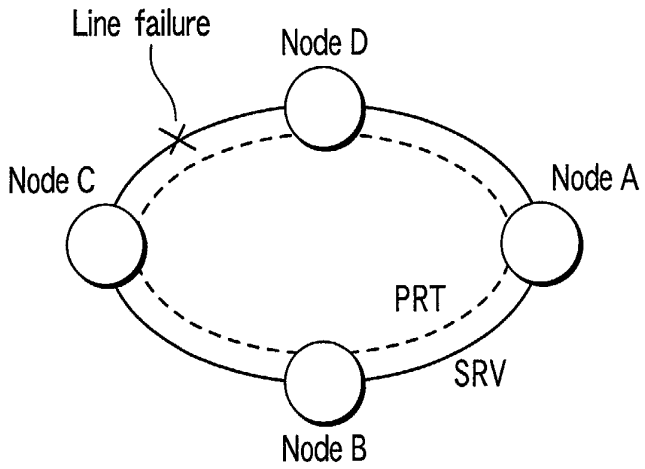
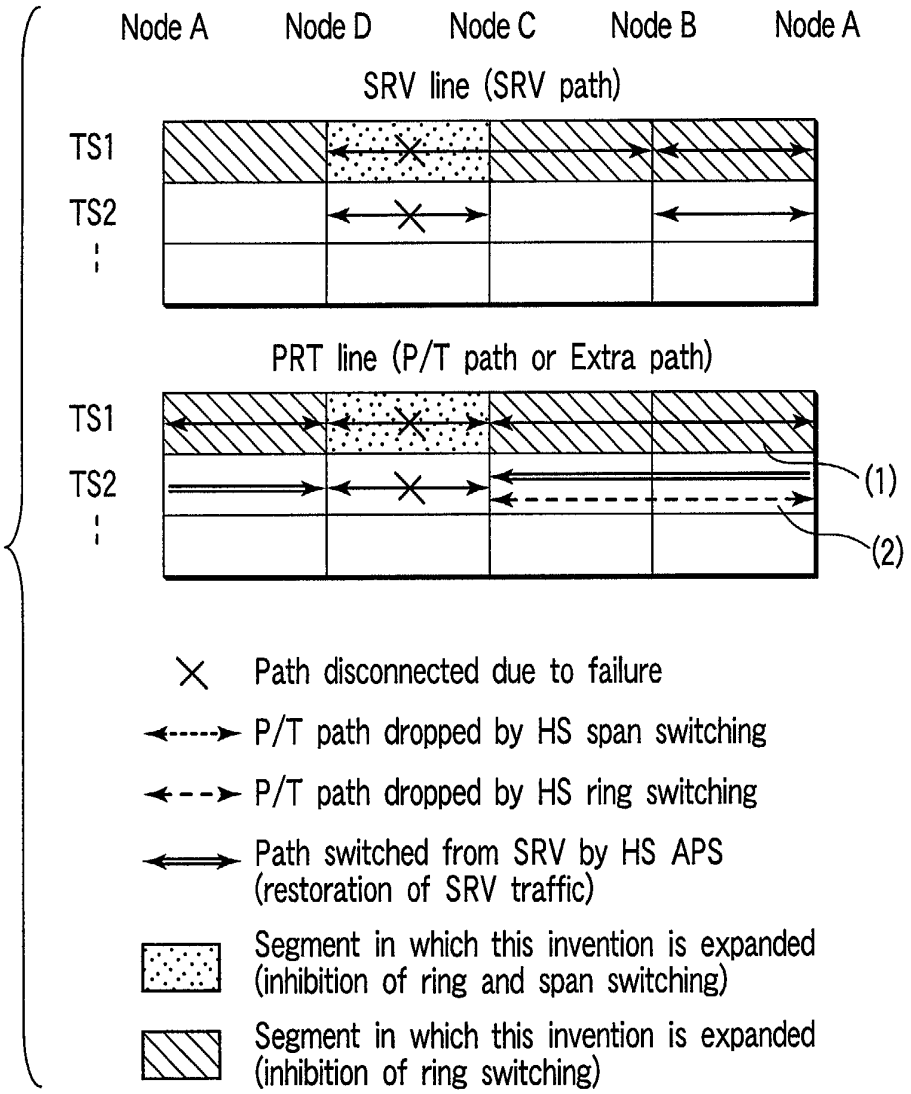

Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 71


Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)

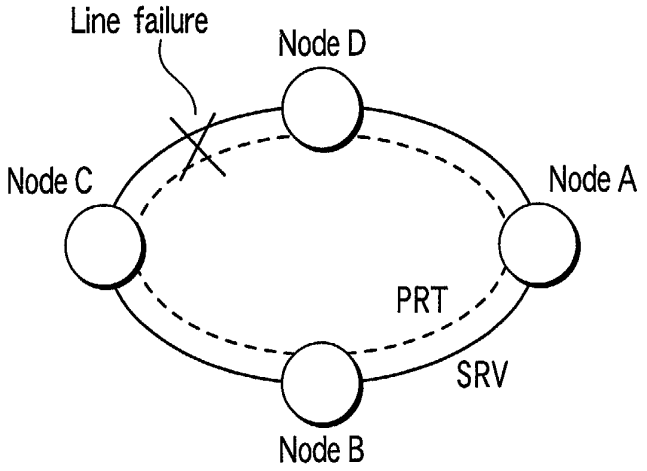
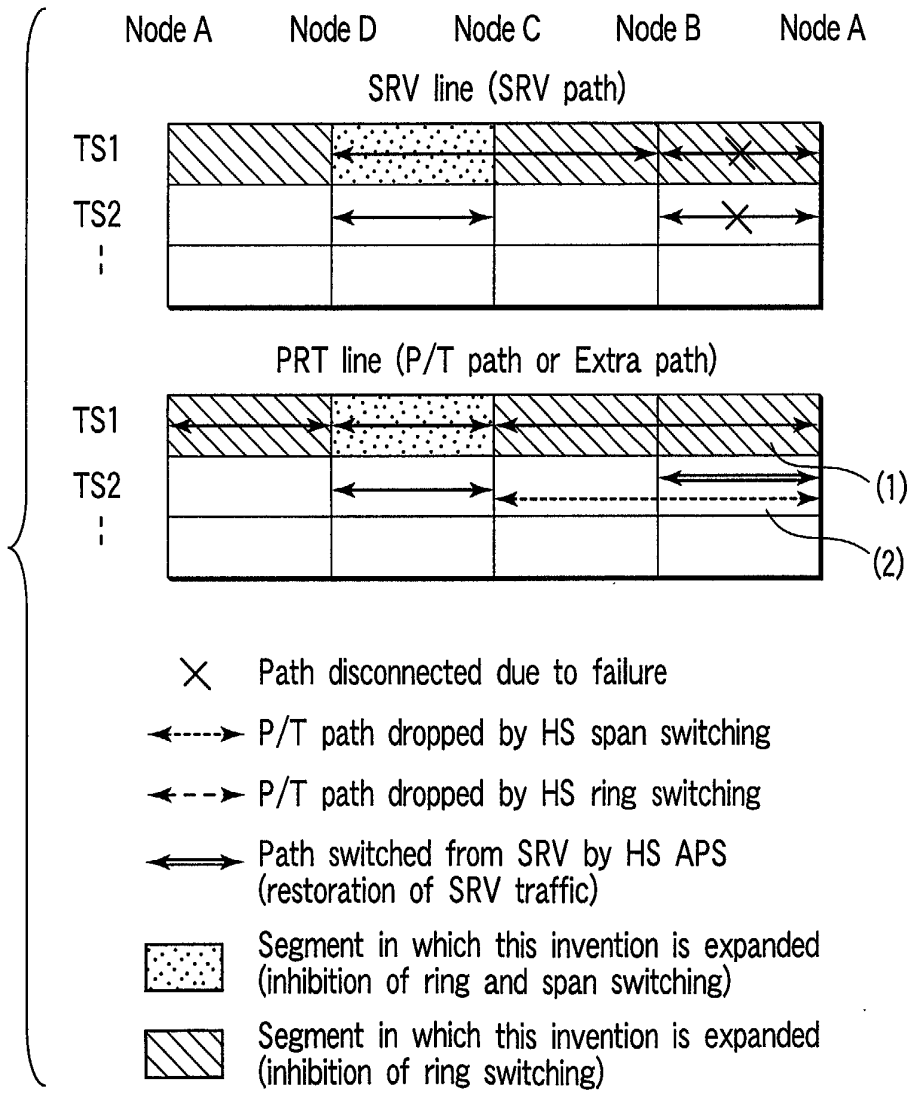

Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 72


Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)

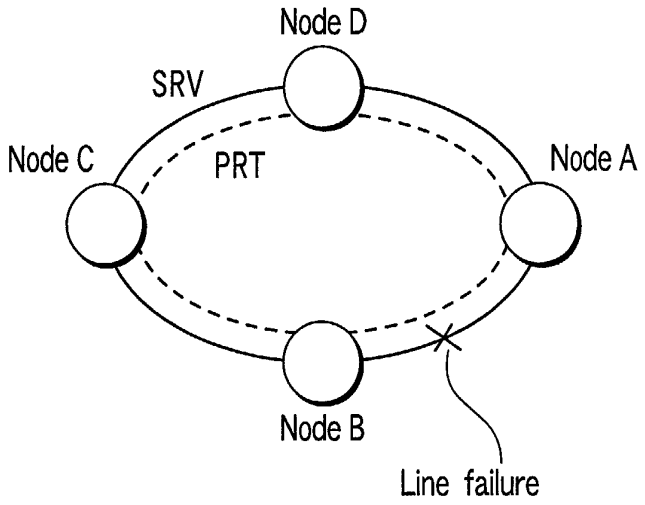
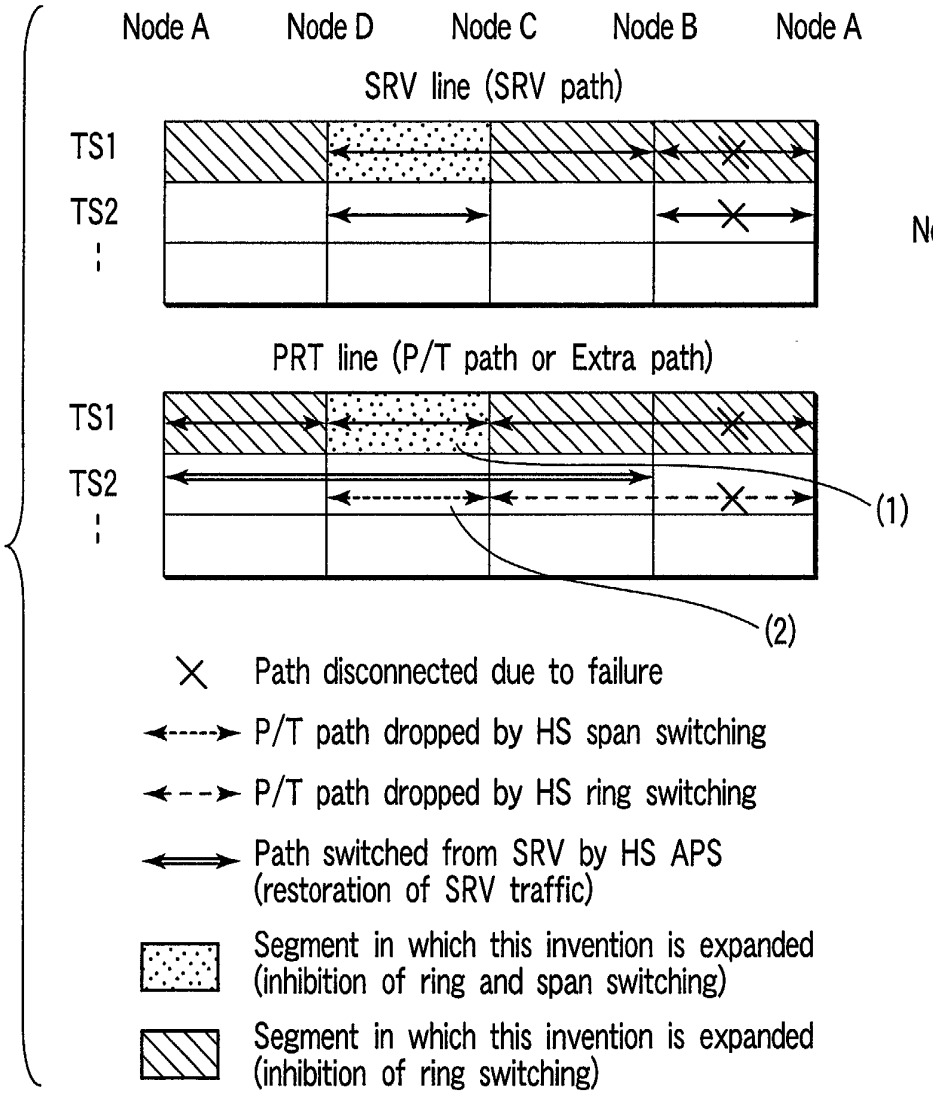

Node D
SRV
Node C
PRT
Node A
Node B
Line failure

FIG. 73


Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
(1)
(2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)

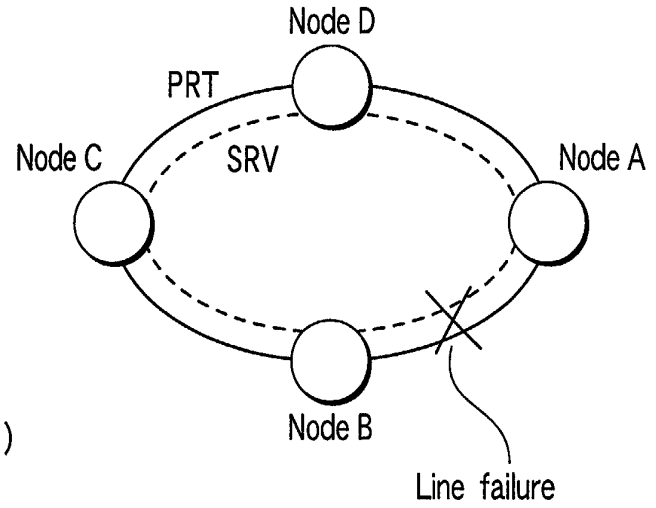

Node D
PRT
Node C
SRV
Node A
Node B
Line failure

FIG. 74

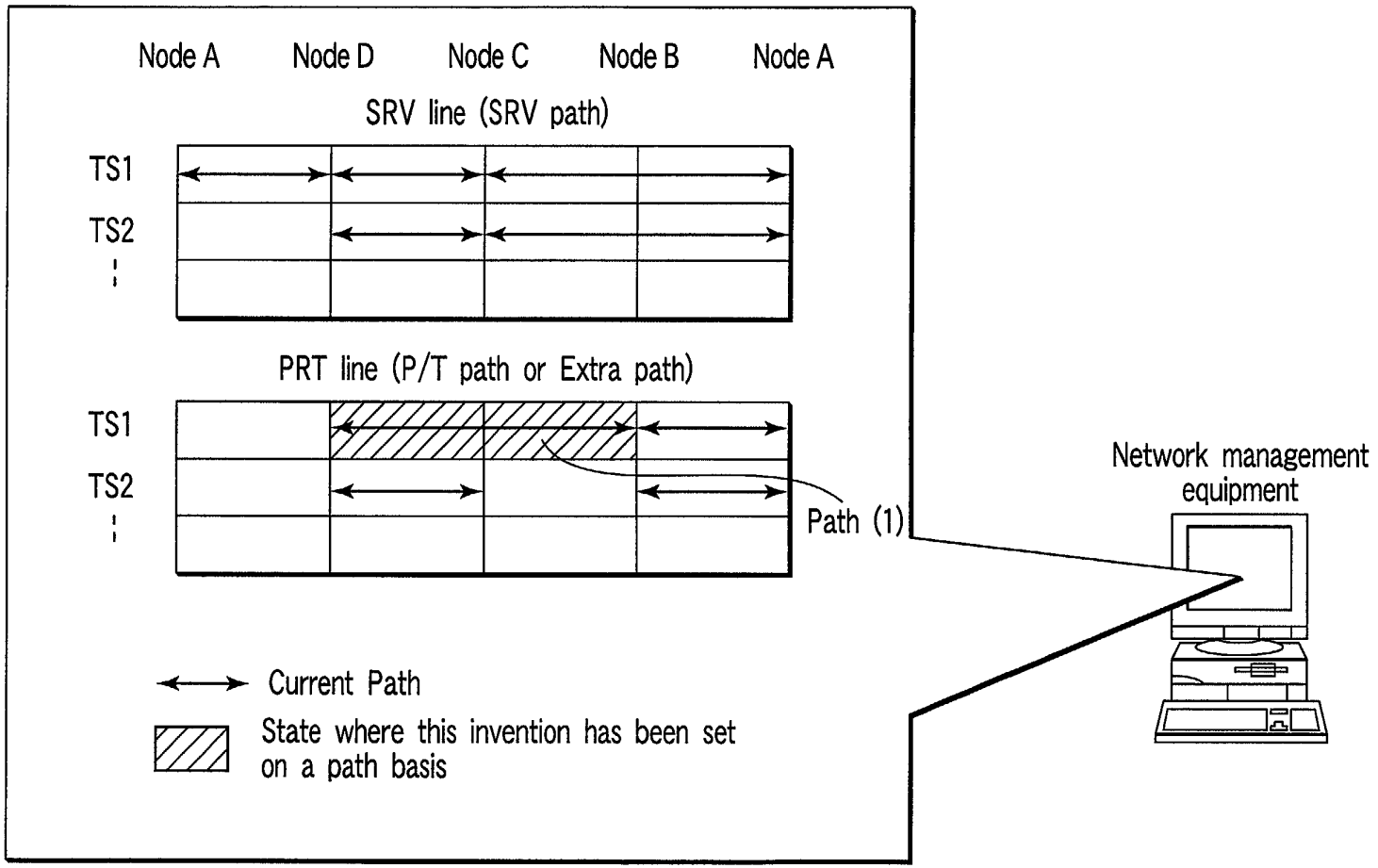

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Path (1)
Network management equipment
Current Path
State where this invention has been set on a path basis

FIG. 75

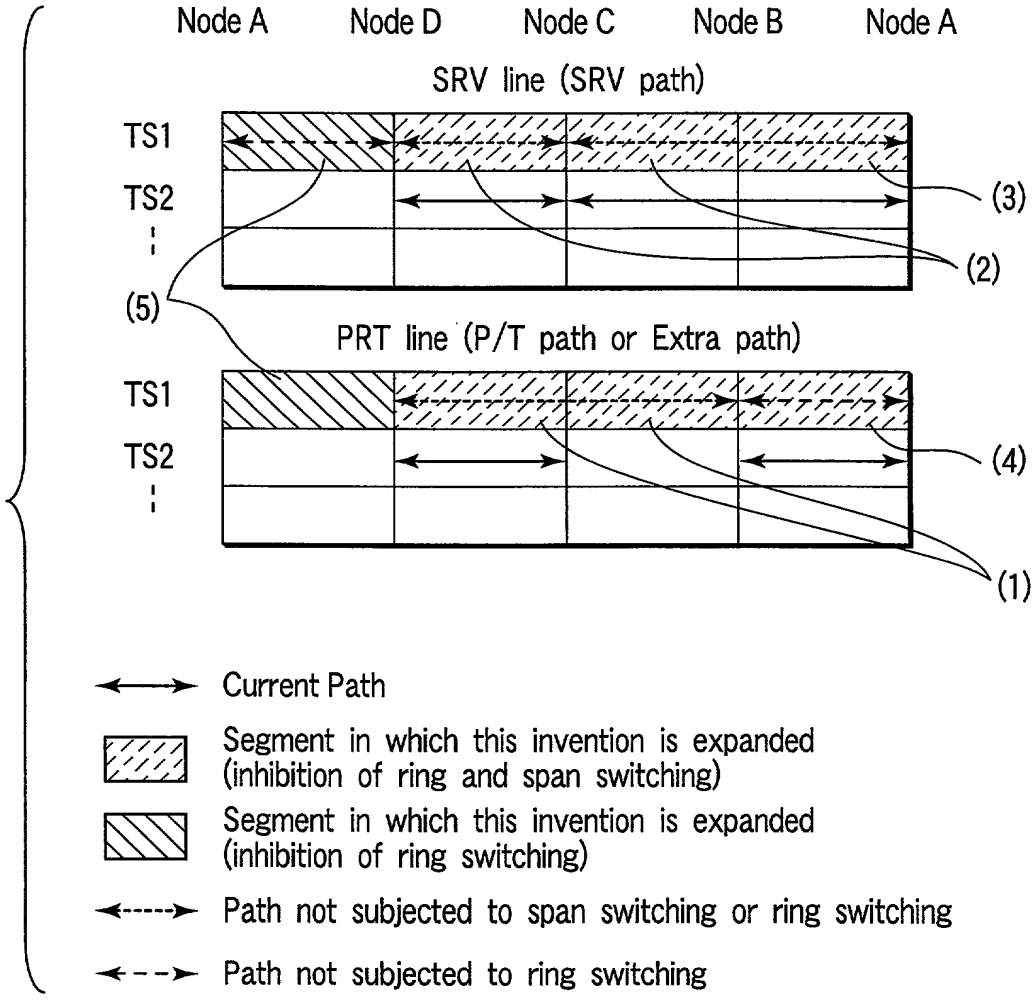

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
(3)
(2)
(5)
PRT line (P/T path or Extra path)
TS1
TS2
(4)
(1)
Current Path
Segment in which this invention is expanded (inhibition of ring and span switching)
Segment in which this invention is expanded (inhibition of ring switching)
Path not subjected to span switching or ring switching
Path not subjected to ring switching

FIG. 76

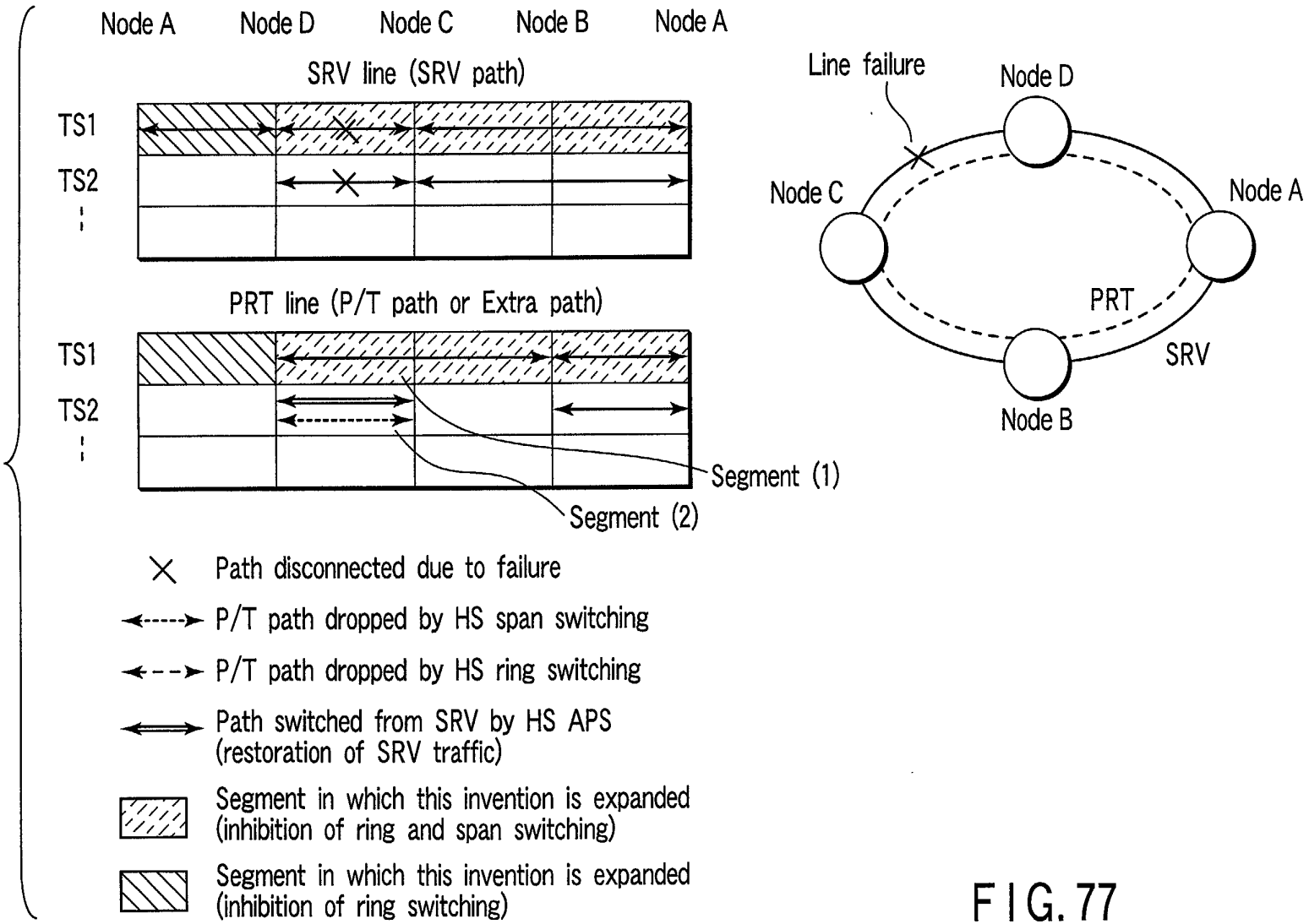


FIG. 77

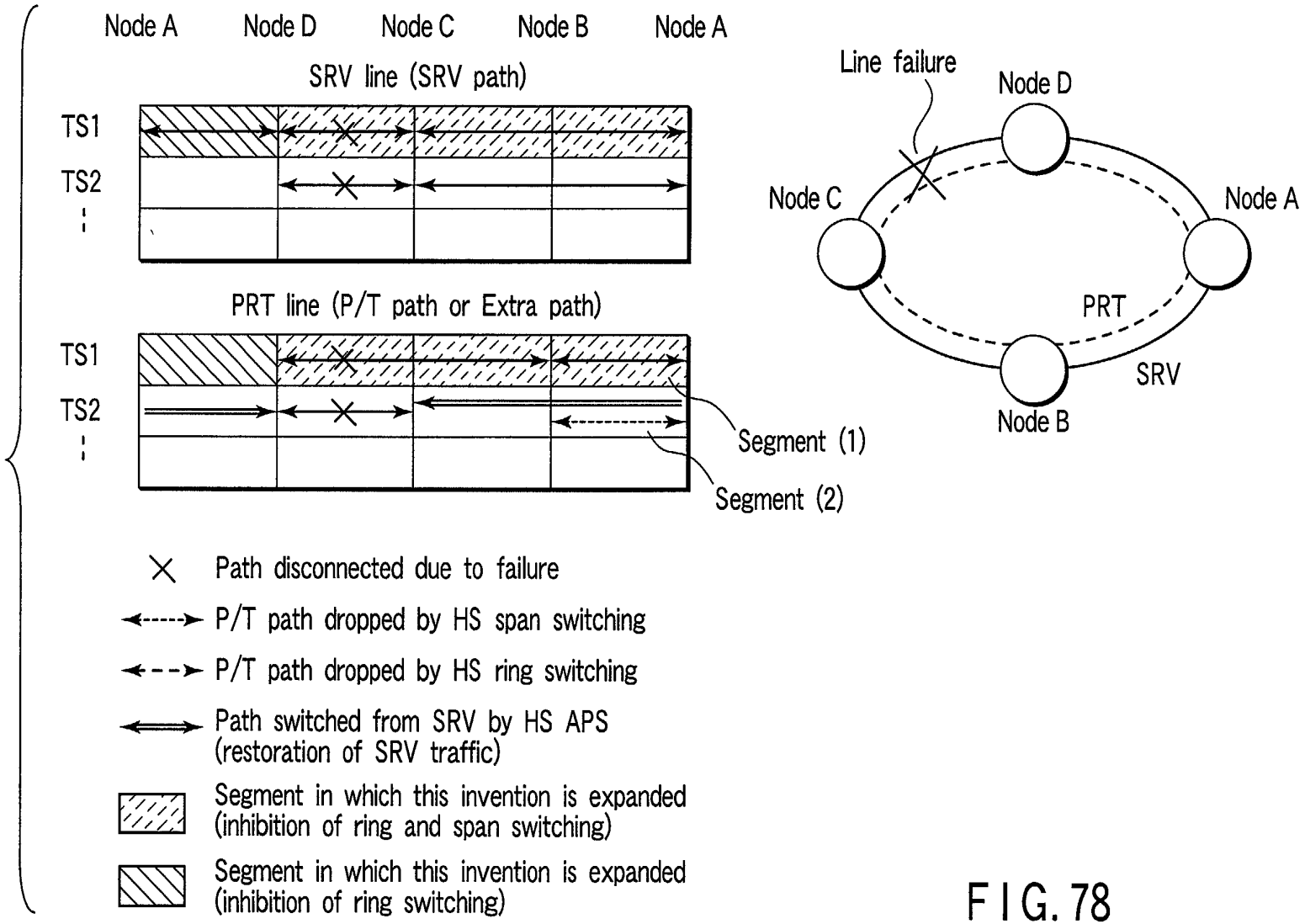

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 78

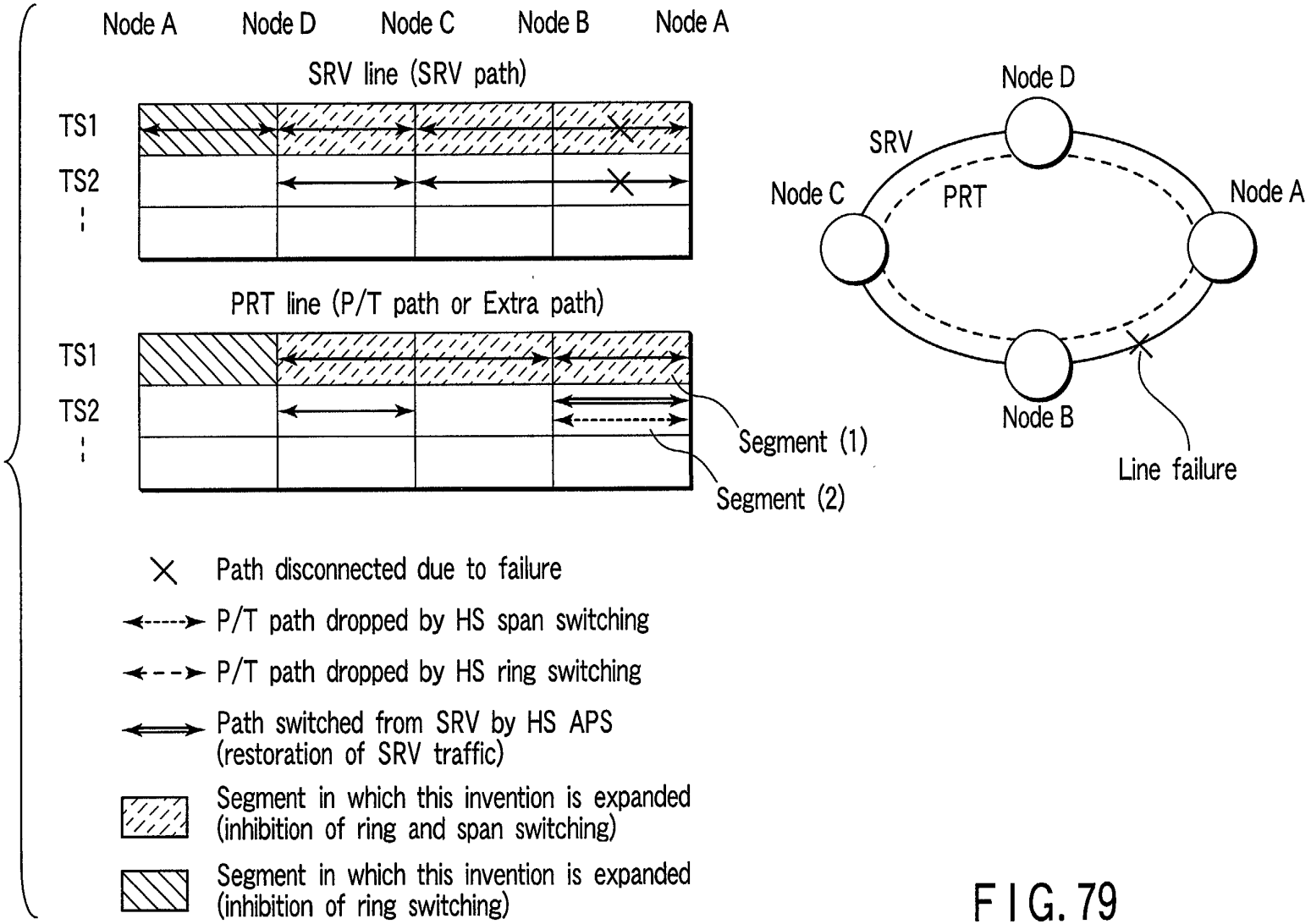

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Node D
SRV
Node C
PRT
Node A
Node B
Line failure
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)

FIG. 79

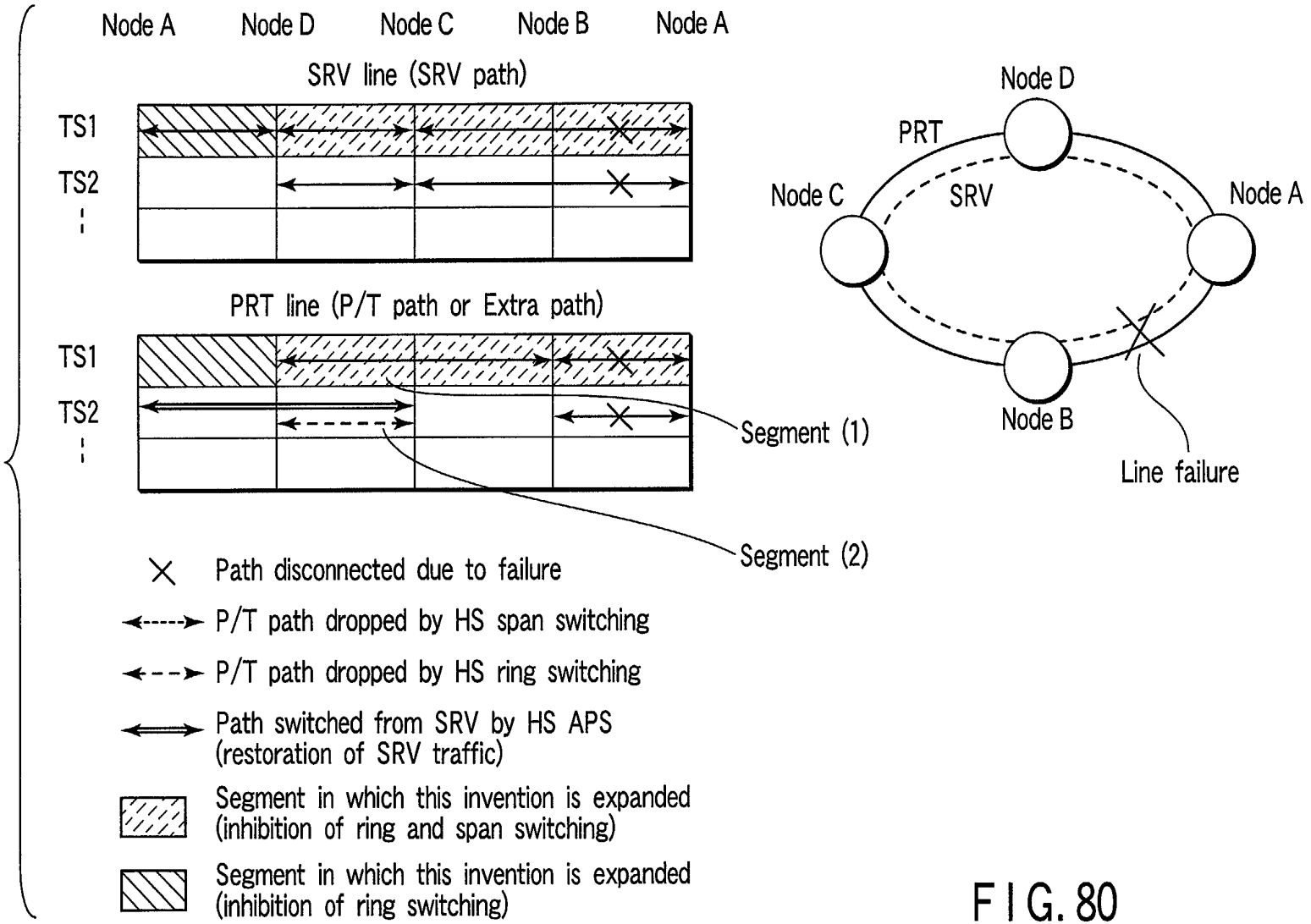

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)
Node D
PRT
Node C
SRV
Node A
Node B
Line failure

FIG. 80

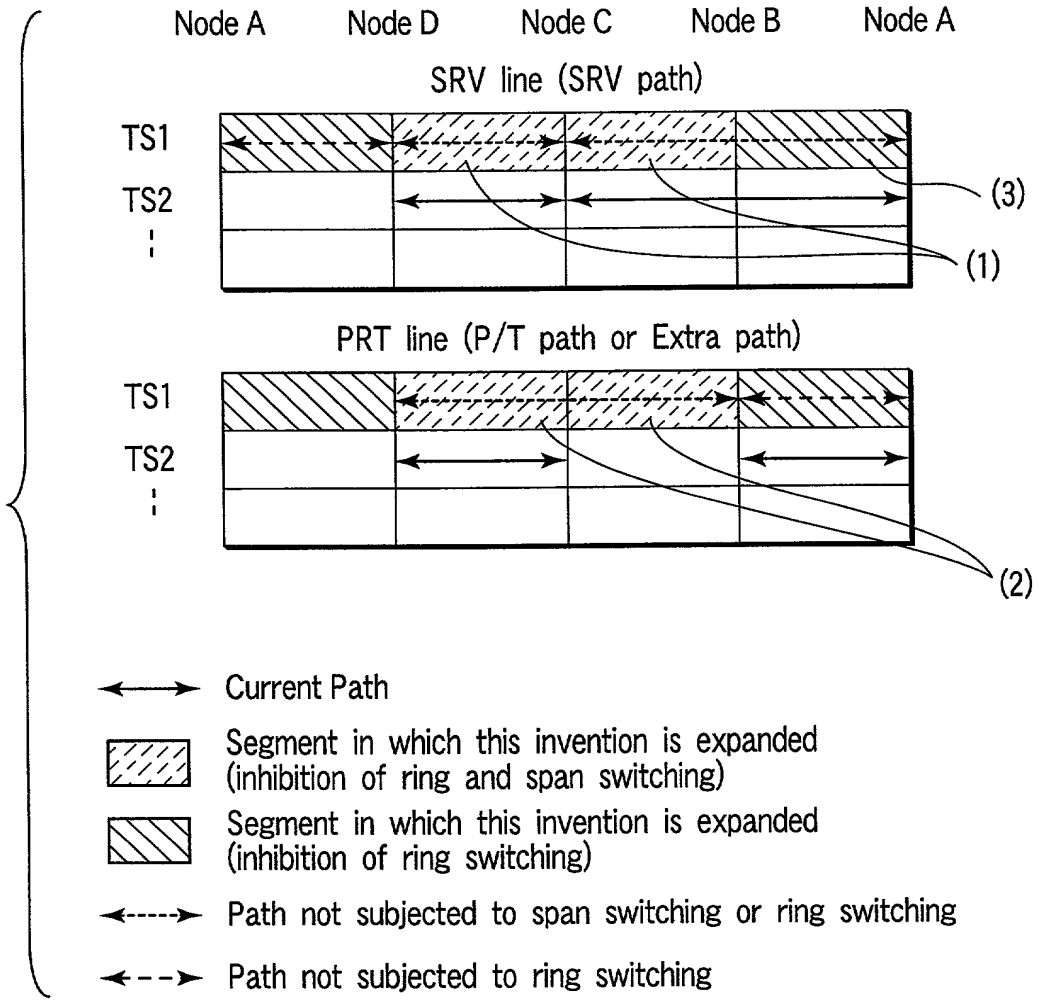

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
(3)
(1)
PRT line (P/T path or Extra path)
TS1
TS2
(2)
Current Path
Segment in which this invention is expanded (inhibition of ring and span switching)
Segment in which this invention is expanded (inhibition of ring switching)
Path not subjected to span switching or ring switching
Path not subjected to ring switching

FIG. 81

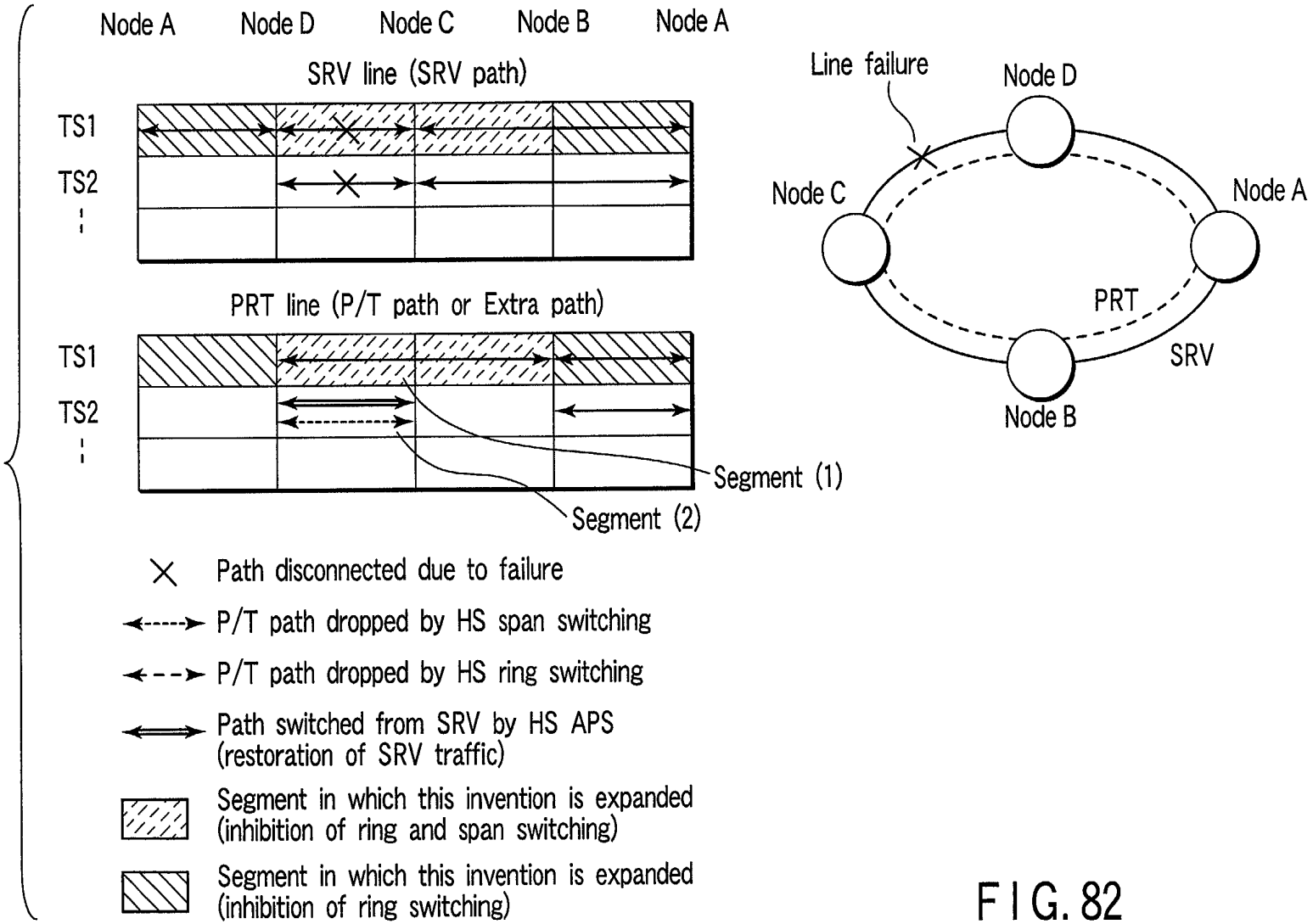

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 82

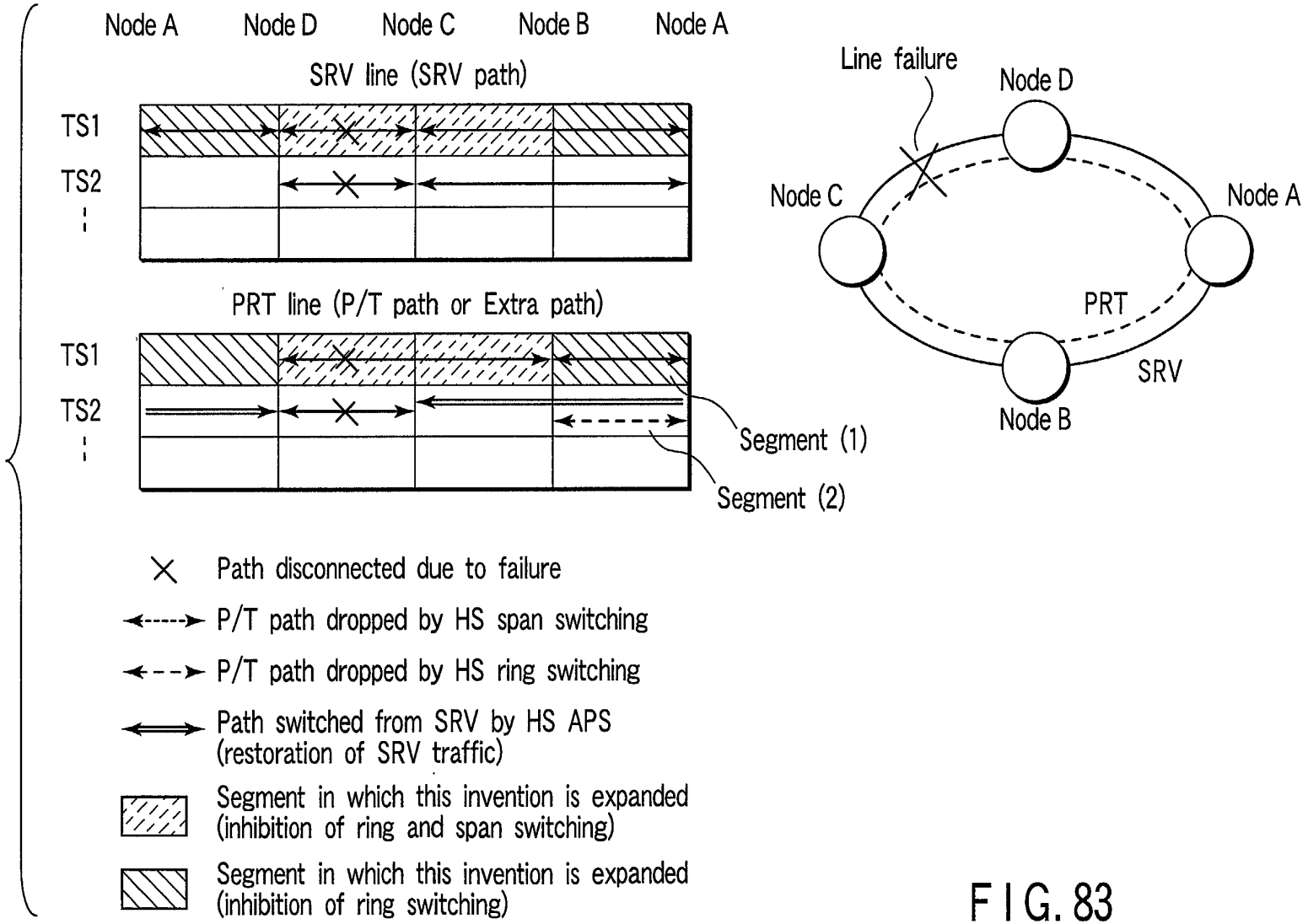

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)
Line failure
Node D
Node C
Node A
PRT
SRV
Node B

FIG. 83

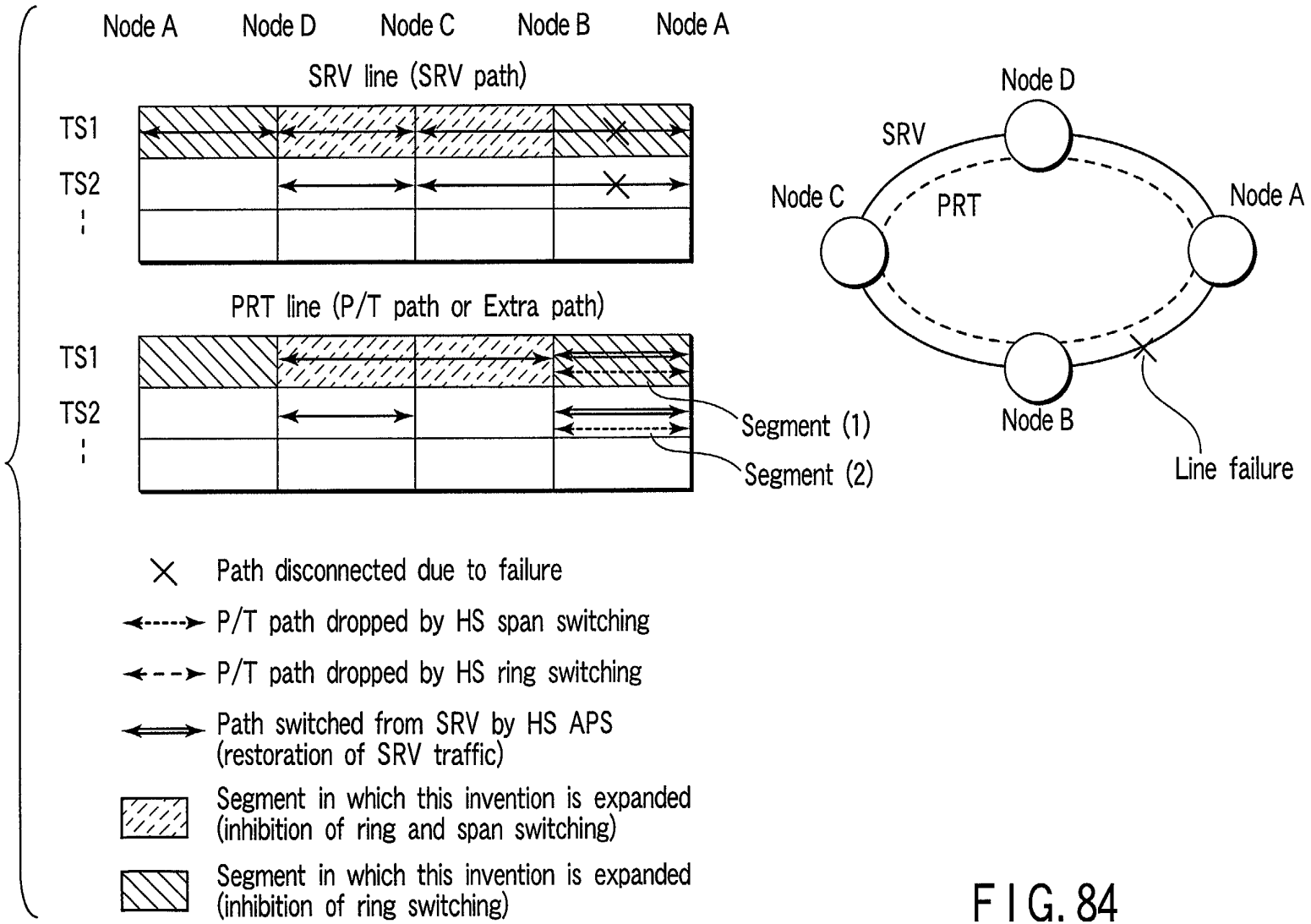

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Node D
SRV
Node C
PRT
Node A
Node B
Line failure
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)

FIG. 84

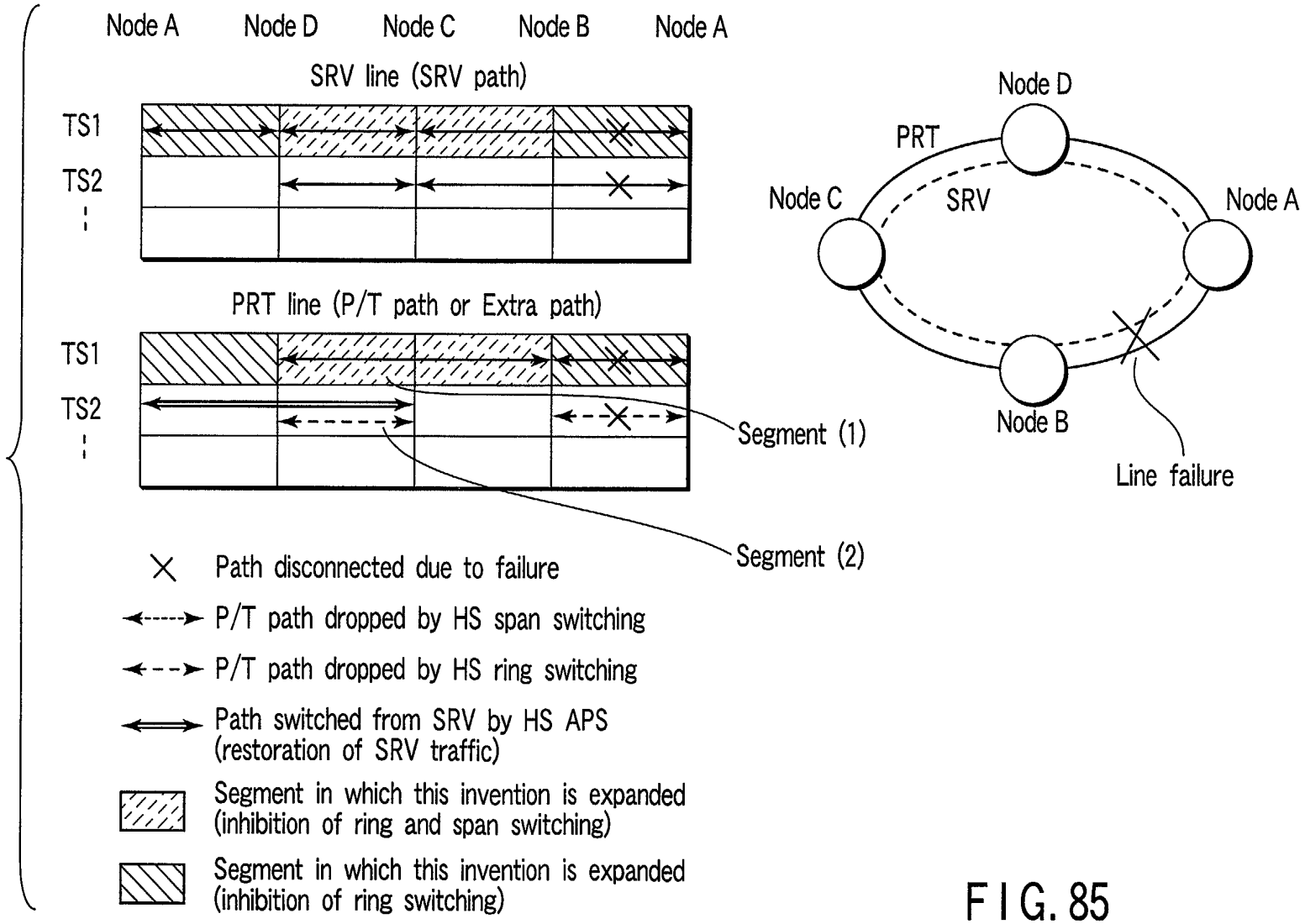

Node A
Node D
Node C
Node B
Node A
SRV line (SRV path)
TS1
TS2
PRT line (P/T path or Extra path)
TS1
TS2
Segment (1)
Segment (2)
Path disconnected due to failure
P/T path dropped by HS span switching
P/T path dropped by HS ring switching
Path switched from SRV by HS APS
(restoration of SRV traffic)
Segment in which this invention is expanded
(inhibition of ring and span switching)
Segment in which this invention is expanded
(inhibition of ring switching)
Node D
PRT
Node C
SRV
Node A
Node B
Line failure

FIG. 85